MU181020A
12.5 Gbit/s PPG
MU181020B
14 Gbit/s PPG
Operation Manual

18th Edition

- **For safety and warning information, please read this manual before attempting to use the equipment.**
- **Additional safety and warning information is provided in the MP1800A Signal Quality Analyzer Installation Guide and the MT1810A 4 Slot Chassis Installation Guide. Please also refer to one of these documents before using the equipment.**
- **Keep this manual with the equipment.**

ANRITSU CORPORATION

Document No.: M-W2752AE-18.0

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Ensure that you clearly understand the meanings of the symbols BEFORE using the equipment. Some or all of the following symbols may be used on all Anritsu equipment. In addition, there may be other labels attached to products that are not shown in the diagrams in this manual.

Symbols used in manual

⚠ DANGER This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.

⚠ WARNING This indicates a hazardous procedure that could result in serious injury or death if not performed properly.

⚠ CAUTION This indicates a hazardous procedure or danger that could result in light-to-severe injury, or loss related to equipment malfunction, if proper precautions are not taken.

Safety Symbols Used on Equipment and in Manual

The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precautions. Ensure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.

This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

This indicates an obligatory safety precaution. The obligatory operation is indicated symbolically in or near the circle.

This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.

These indicate that the marked part should be recycled.

MU181020A 12.5 Gbit/s PPG
MU181020B 14 Gbit/s PPG
Operation Manual

20 December 2006 (First Edition)
10 July 2015 (18th Edition)

Equipment Certificate

Anritsu Corporation certifies that this equipment was tested before shipment using calibrated measuring instruments with direct traceability to public testing organizations recognized by national research laboratories, including the National Institute of Advanced Industrial Science and Technology, and the National Institute of Information and Communications Technology, and was found to meet the published specifications.

Anritsu Warranty

Anritsu Corporation will repair this equipment free-of-charge if a malfunction occurs within one year after shipment due to a manufacturing fault. However, software fixes will be made in accordance with the separate Software End-User License Agreement. Moreover, Anritsu Corporation will deem this warranty void when:

- The fault is outside the scope of the warranty conditions separately described in the operation manual.
- The fault is due to mishandling, misuse, or unauthorized modification or repair of the equipment by the customer.
- The fault is due to severe usage clearly exceeding normal usage.
- The fault is due to improper or insufficient maintenance by the customer.
- The fault is due to natural disaster, including fire, wind, flooding, earthquake, lightning strike, or volcanic ash, etc.
- The fault is due to damage caused by acts of destruction, including civil disturbance, riot, or war, etc.
- The fault is due to explosion, accident, or breakdown of any other machinery, facility, or plant, etc.
- The fault is due to use of non-specified peripheral or applied equipment or parts, or consumables, etc.
- The fault is due to use of a non-specified power supply or in a non-specified installation location.
- The fault is due to use in unusual environments(Note).
- The fault is due to activities or ingress of living organisms, such as insects, spiders, fungus, pollen, or seeds.

In addition, this warranty is valid only for the original equipment purchaser. It is not transferable if the equipment is resold.

Anritsu Corporation shall assume no liability for injury or financial loss of the customer due to the use of or a failure to be able to use this equipment.

Note:
For the purpose of this Warranty, "unusual environments" means use:

- In places of direct sunlight
- In dusty places
- Outdoors
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
- In places where condensation occurs
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes

Anritsu Corporation Contact

In the event of this equipment malfunctions, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

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Before re-exporting the product or manuals, please contact us to confirm whether they are export-controlled items or not.

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   iv) If this Software or the Equipment has been modified, repaired, or otherwise altered without Anritsu's prior approval.
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Anritsu shall deem this EULA terminated if you violate any conditions described herein. This EULA shall also be terminated if the conditions herein cannot be continued for any good reason, such as violation of copyrights, patents, or other laws and ordinances.

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If Anritsu suffers any loss, financial or otherwise, due to your violation of the terms of this EULA, Anritsu shall have the right to seek proportional damages from you.

7. Responsibility after Termination

Upon termination of this EULA in accordance with item 5, you shall cease all use of this Software immediately and shall as directed by Anritsu either destroy or return this Software and any backup copies, full or partial, to Anritsu.

8. Dispute Resolution

If matters of dispute or items not covered by this EULA arise, they shall be resolved by negotiations in good faith between you and Anritsu.

9. Court of Jurisdiction

This EULA shall be interpreted in accordance with Japanese law and any disputes that cannot be resolved by negotiation described in Article 8 shall be settled by the Japanese courts.

CE Conformity Marking

Anritsu affixes the CE Conformity marking on the following product(s) in accordance with the Council Directive 93/68/EEC to indicate that they conform to the EMC and LVD directive of the European Union (EU).

CE marking

1. Product Model

Plug-in Units: MU181020A 12.5 Gbit/s PPG
MU181020B 14 Gbit/s PPG

2. Applied Directive and Standards

When the MU181020A 12.5 Gbit/s PPG or MU181020B 14 Gbit/s PPG is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU181020A/B can be used with.

C-Tick Conformity Marking

Anritsu affixes the C-Tick marking on the following product(s) in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

C-Tick marking

1. Product Model

Plug-in Units: MU181020A 12.5 Gbit/s PPG
MU181020B 14 Gbit/s PPG

2. Applied Directive and Standards

When the MU181020A 12.5 Gbit/s PPG or MU181020B 14 Gbit/s PPG is installed in the MP1800A or MT1810A, the applied directive and standards of this unit conform to those of the MP1800A or MT1810A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU181020A/B can be used with.

About This Manual

A testing system combining an MP1800A Signal Quality Analyzer or MT1810A 4-Slot Chassis mainframe, module(s), and control software is called a Signal Quality Analyzer Series. The operation manuals of the Signal Quality Analyzer Series consist of separate documents for the installation guide, the mainframe, remote control operation, module(s), and control software, as shown below.

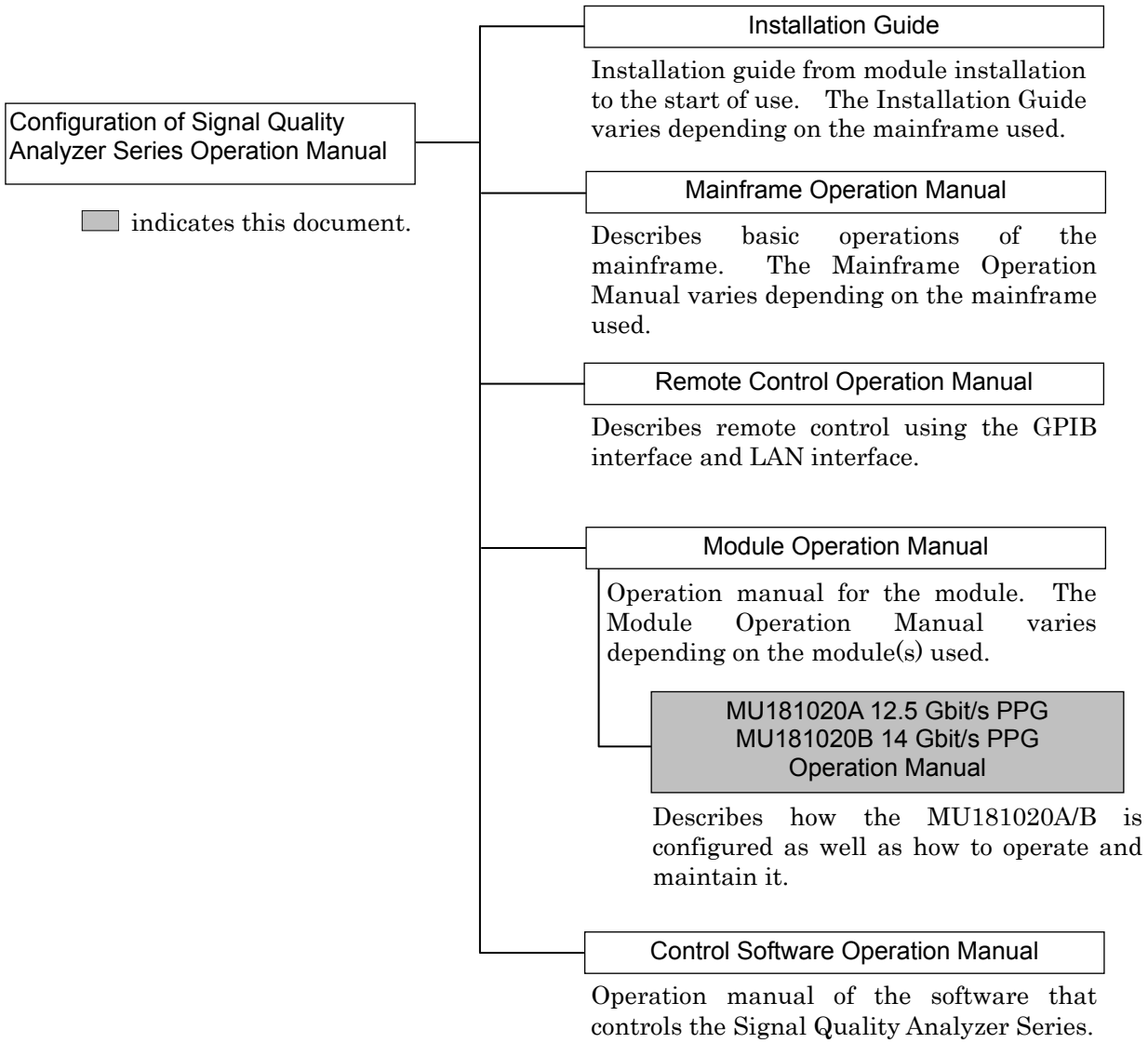


Table of Contents

Chapter 1 Overview

This chapter provides an overview of the MU181020A 12.5 Gbit/s PPG and the MU181020B 14 Gbit/s PPG (hereinafter, referred to as "MU181020A/B").
This document only explains the MU181020A, unless there is a special item.

1.1 Product Overview

The MU181020A is a plug-in module that can be built into a Signal Quality Analyzer mainframe. It can generate a variety of patterns within the operating frequency range, including PRBS, DATA, Zero-Substitution, Alternate, Mixed, and Sequence patterns.

Various option configurations are available for the MU181020A. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

Features of the MU181020A:

- Capable of generating PRBS, DATA, Zero-Substitution, Alternate, Mixed, and Sequence patterns.
- Provides a large amount of user-programmable patterns (128 Mbits)
- Supports a variety of applications such as research, development, and production of devices, by installing options.
- Flexible for functional expansion in the future, by installing additional options.
- Devices up to 25Gbit/s can be evaluated using two MU181020A modules and up to 28Gbit/s using two MU181020B modules.
- Devices up to 50Gbit/s can be evaluated using four MU181020A modules and up to 56Gbit/s using four MU181020B modules.

1.2 Product Composition

1.2.1 Standard composition

Table 1.2.1-1 and Table 1.2.1-2 show the standard compositions of the MU181020A/B.

Table 1.2.1-1 Standard composition of MU181020A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU181020A	12.5Gbit/s PPG	1	
Accessories	Z0897A	MP1800A Manual CD	1	CD-ROM version
	J1137	Terminator	3	
	J1341A	Open	1	
	Z0918A	MX180000A Software CD	1	CD-ROM version

Table 1.2.1-2 Standard composition of MU181020B

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU181020B	14Gbit/s PPG	1	
Accessories	Z0897A	MP1800A Manual CD	1	CD-ROM version
	J1137	Terminator	3	
	J1341A	Open	1	
	Z0918A	MX180000A Software CD	1	CD-ROM version

1.2.2 Options

Table 1.2.2-1, Table 1.2.2-2, Table 1.2.2-3 and Table 1.2.2-4 show the options for the MU181020A/B. All options are sold separately.

Table 1.2.2-1 Options of MU181020A

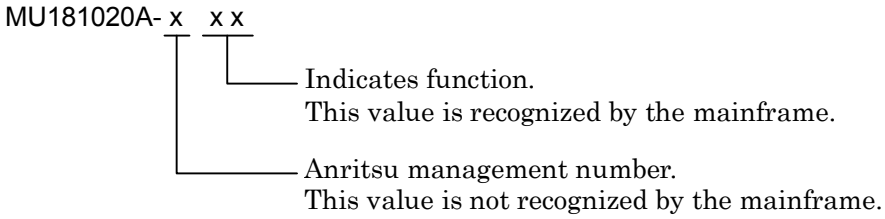
Model name	Product name	Remarks
MU181020A-001	9.8 to 12.5 Gbit/s	Cannot be installed together with MU181020A-002.
MU181020A-002	0.1 to 12.5 Gbit/s	Cannot be installed together with MU181020A-001.
MU181020A-x10	Variable Data Output (0.05 to 0.8 Vp-p)	Cannot be installed together with MU181020A-x11 and MU181020A-x12 and MU181020A-x13.
MU181020A-x11	Variable Data Output (0.25 to 2.5 Vp-p)	Cannot be installed together with MU181020A-x10 and MU181020A-x12 and MU181020A-x13.
MU181020A-x12	High Performance Data Output (0.05 to 2.0 Vp-p)	Cannot be installed together with MU181020A-x10 and MU181020A-x11 and MU181020A-x13.
MU181020A-x13	Variable Data Output (0.5 to 3.5 Vp-p)	Cannot be installed together with MU181020A-x10 and MU181020A-x11 and MU181020A-x12.
MU181020A-x21	Differential Clock Output (0.1 to 2.0 Vp-p)	
MU181020A-x30	Variable Data Delay	Cannot be installed into MU181020A-001.

Table 1.2.2-2 Options for MU181020B

Model name	Product name	Remarks
MU181020B-002	0.1 to 14 Gbit/s	Necessary option
MU181020B-003*1	14.05 Gbit/s Extension	
MU181020B-005*1	14.1Gbit/s Extension	
MU181020B-x11	Variable Data Output (0.25 to 2.5 Vp-p)	Cannot be installed together with MU181020B-x12 and MU181020B-x13.
MU181020B-x12	High Performance Data Output (0.05 to 2.0 Vp-p)	Cannot be installed together with MU181020B-x11 and MU181020B-x13.
MU181020B-x13	Variable Data Output (0.5 to 3.5 Vp-p)	Cannot be installed together with MU181020B-x11 and MU181020B-x12.
MU181020B-x21	Differential Clock Output (0.1 to 2.0 Vp-p)	
MU181020B-x30	Variable Data Delay	

Note:

Option name format is as follows:



*1: Notes on MU181020B Option Model Display
The model and name of the MU181020B-003 and -005 option are recorded on the front panel of each module. Although the screen displaying the option details using software indicates MU181020B-02 (0.1 to 14 Gbit/s) the assured operating bit rates are actually 0.1 to 14.05 Gbit/s or 0.1 to 14.1 Gbit/s.

Table 1.2.2-3 Standard Accessories of MU181020A Options

Applicable Option	Model name/symbol	Product name	Q'ty	Remarks
MU181020A-x11, x12, x13, x21	J1359A	Coaxial adapter (compatible among K-P, K-J, and SMA)	2	
MU181020A-x21	J1137	Terminator	1	

Table 1.2.2-4 Standard Accessories of MU181020B Options

Applicable Option	Model name/symbol	Product name	Q'ty	Remarks
MU181020B-x11, x12, x13, x21	J1359A	Coaxial adapter (compatible among K-P, K-J, and SMA)	2	
MU181020B-x21	J1137	Terminator	1	

1.2.3 Application parts

Table 1.2.3-1 and Table 1.2.3-2 show the application parts for the MU181020A/B. All application parts are sold separately.

Table 1.2.3-1 Application parts for MU181020A

Model name/ symbol	Product name	Remarks
J1360A	Measurement kit	Coaxial cable 0.8 m × 2 Coaxial cable 1.0 m × 1
J1343A	Coaxial cable (1 m)	SMA connector
J1342A	Coaxial cable (0.8 m)	APC3.5 connector
J1137	Terminator	
J1359A	Coaxial adapter (compatible among K-P, K-J, and SMA)	
W2752AE	Operation manual	Printed version
Z0306A	Wrist strap	
J1678A	ESD Protection Adapter-K	K connector

Table 1.2.3-2 Application parts for MU181020B

Model name/ symbol	Product name	Remarks
J1360A	Measurement kit	Coaxial cable 0.8 m × 2 Coaxial cable 1.0 m × 1
J1343A	Coaxial cable (1 m)	SMA connector
J1342A	Coaxial cable (0.8 m)	APC3.5 connector
J1137	Terminator	
J1359A	Coaxial adapter (compatible among K-P, K-J, and SMA)	
W2752AE	Operation manual	Printed version
Z0306A	Wrist strap	
J1678A	ESD Protection Adapter-K	K connector

1.3 Specifications

1.3.1 Specifications for MU181020A

Table 1.3.1-1 Specifications for MU181020A

Item	Specifications	Remarks
Operating frequency range	9.8 to 12.5 GHz	When MU181020A-001 is installed
Operating bit rate	9.8 to 12.5 Gbit/s (1/1 Mode)	
	4.9 to 6.25 Gbit/s (1/2 Mode)	
	2.45 to 3.125 Gbit/s (1/4 Mode)	
	1.225 to 1.5625 Gbit/s (1/8 Mode)	
Input switching	Can be switched between Internal and External.	
Internal clock		
Frequency variable range	9.8 to 12.5 GHz (1/1 Mode)	
	4.9 to 6.25 GHz (1/2 Mode)	
	2.45 to 3.125 GHz (1/4 Mode)	
	1.225 to 1.5625 GHz (1/8 Mode)	
Resolution	1-kHz/1-MHz steps	
Signal purity	–75 dBc/Hz (Typ.) SSB phase noise (10-kHz offset, bandwidth: 1 Hz)	
External clock		
Input frequency	9.8 to 12.5 GHz bit rate, 1/1 clock or 1/64 clock	
Input signal purity	1/1 clock (9.8 to 12.5 GHz) <–90 dBc/Hz 1/64 clock (153.125 to 195.3125 MHz) <–110 dBc/Hz SSB phase noise (10-kHz offset, bandwidth: 1 Hz)	
External clock		When MU181020A-002 is installed
Operating frequency range	0.1 to 12.5 GHz	
Pattern generation	Repeat/Burst	
Data Sequence	Restart/Consecutive/Continuous	When Burst is set

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Generated pattern			
PRBS	Pattern length	2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Mark ratio	1/2, 1/4, 1/8, 0/8, 1/2INV, 3/4, 7/8, 8/8	
	Number of AND bit shifts at the mark ratio	1 bit/3 bits (at 1/4, 3/4, 7/8, 1/8)	
Zero-Substitution	Pattern length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)	
	Successive-zeros bit length	1 to (pattern length – 1) bits can be inserted.	
Data	Pattern length	2 to 134, 217, 728 bits, in 1-bit steps In the case of 2 Ch Combination: 4 to 268 435 456 bits, in 2-bit steps In the case of 4 Ch Combination: 8 to 536 870 912 bits, in 4-bit steps	
Alternate	Pattern length	128 to 67 108 864 bits, in 128-bit steps Can be set independently for patterns A and B.	Cannot be set when Combination or Burst is set.
	Loop Control	Internal, External, Manual (1 shot, asynchronous)	
	Loop Time	1 to 511 times, in 1-time steps Can be set independently for patterns A and B.	
Mixed	Loop Control	Alternate switching control	
	Loop Time	1 to 511 times, in 1-time steps Can be set independently for patterns A and B.	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Mixed (continued)	Number of blocks	1 to the smallest number among a to d, below, in 1-block steps a) 511 b) INT (128 Mbits × x/(Number of rows × Data Length')) where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT (Data Length/(128 × x)) +1) × 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of blocks fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31}) × x/(Row Length × Number of rows)) where x is: 1 for Independent 2 for 2 Ch Combination 4 for 4 Ch Combination d) (Row Length – Data Length) × Number of blocks ≥ 2^31(2 147 483 648)	
	Pattern	Data, Alternate (Alternate cannot be set for Combination.)	
	Data Length	512 to 134 217 728 bits (Data) 512 to 67 108 864 bits (Alternate) In the case of 2 Ch Combination 1 024 to 268 435 456 bits, in 2-bit steps (Data) In the case of 4 Ch Combination 2 048 to 536 870 912 bits, in 4-bit steps (Data) PRBS length: $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Row Length	768 to 2 281 701 376 bits, in 128-bit steps (Data) 768 to 2 214 592 512 bits, in 128-bit steps (Alternate) In the case of 2 Ch Combination: 1 536 to 4 563 402 752 bits, in 256-bit steps (Data) In the case of 4 Ch Combination: 3 072 to 9 126 805 504 bits, in 512-bit steps (Data)	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Mixed (continued)	Number of rows	1 to the smallest number among a to c, below, in 1-row steps a) 16 b) INT (128 Mbit × x/Data Length') where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT(Data Length/(128 × x))+1)× 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of rows fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31})× x/Row Length) where x is; 1 in the case of Independent 2 in the case of 2 Ch Combination 4 in the case of 4 Ch Combination	
Sequence	Block number	1 to 128/1 Step	Cannot be set when Combination or Burst is set.
	Block length	8 192 to 1 048 576 bits, in 128-bit steps	
	Loop time	1 to 1 024 times, in 1-time steps, or repeat	
	Sequence conditions	Can be set independently for each block. A pattern match, B pattern match, Manual, Trigger, loop complete, External trigger	
	Next destination	Next, Stop, Jump, None	
Pattern Sequence	Repeat	Continuous Pattern	
	Burst	Burst Pattern (supports PRBS, Zero-Substitution, Data and Mixed) Source: Internal, External-Trigger (AUX Input), External-Enable (AUX Input) Data Sequence: Restart, Consecutive, Continuous Burst Cycle: 1 280 to 2 147 483 648 bits / 128 bits step Enable period: 640 to 2 147 483 520 bits / 128 bits	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Logical inversion		Can be switched between Positive and Negative.	
Error addition	Area	ALL, Specific block (Can be selected only for ALTN, Mixed and Sequence.)	
	Control Method	Can be switched among Internal, External-Trigger and External-Disable. (Use AUX input for external input.)	
	Error Variation	Repeat, Single	
	Error Ratio	*E–n (* = 1 to 9, n = 2 to 12)	n=3 to 12 when Combination is set.
	Insertion CH	1 to 32, CH Scan (Only when Internal is set.)	
External clock input	Input frequency range	1/1 Clock: 9.8 to 12.5 GHz	When MU181020A-001 is installed
		1/64 Clock: 153.125 to 195.3125 MHz	
		0.1 to 12.5 GHz	When MU181020A-002 is installed
	Input amplitude	0.4 to 2.0 Vp-p (–4 to 10 dBm)	
	Input waveform	100 to 500 MHz: Rectangular wave > 500 MHz: Sine wave or rectangular wave (Duty: 50%)	
	Termination	AC/50 Ω	
	Connector	SMA	
AUX input	Input signal selection	Alternate Control (L: pattern A, H: pattern B) When Alternate or Mixed-Alternate is selected as the generated pattern.	
		Sequence Control (transits to the next sequence at rising edge detection) When Sequence is selected as the generated pattern.	
		Error Injection (error occurs at rising edge detection) In the case of 2 or 4 Ch Combination, input only to Master Module is enabled.	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
AUX input (continued)	Input signal selection (continued)	Burst: When Burst is set in Pattern Sequence, and Source is set to other than Internal. In the case of 2 or 4 Ch Combination, input only to Master Module is enabled. External Trigger (data occurs at rising edge detection) External Enable (L: Data disable, H: Data enable)	
	Minimum pulse width	1/64 of data rate	
	Input level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Termination	50 Ω/GND	
	Connector	SMA	
AUX output	Output signal selection	1/N Clock Pattern Sync/Burst Output2 Burst Output2 is enabled when Burst is set in Pattern Sequence.	
	1/N Clock	1/N: N = 2, 4, 8, 9, 10…510, 511	When MU181020A -002 is installed
		1/N: N = 2, 4, 8, 9, 10…510 511 (1/1 Mode)	When MU181020A -001 is installed
		1/N: N = 1, 2, 4, 8, 9, 10…254, 255 (1/2 Mode)	
		1/N: N = 1, 2, 4, 8, 9, 10…126, 127 (1/4 Mode)	
		1/N: N = 1, 2, 4, 8, 9, 10…62, 63 (1/8 Mode)	
	Pattern Sync		
	When PRBS, Data or Zero-substitution is set	Position: 1 to {(Least common multiple of Pattern Length*1 and 64) –79}, in 16-bit steps The maximum settable number is 68 719 476 657. In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length*1 and 128) – 159}, in 32-bit steps In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length*1 and 256) – 319}, in 64-bit steps The maximum settable number is 274 877 906 625.	

*1: At Independent, when the pattern length is 127 bits or less, specify the length as an integer multiple so that it becomes 128 bits or more.
At 2 Ch Combination, when the pattern length is 255 bits or less, specify the length as an integer multiple so that it becomes 256 bits or more.
At 4 Ch Combination, when the pattern length is 511 bits or less, specify the length as an integer multiple so that it becomes 512 bits or more.

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
AUX output (continued)	When Alternate is set	Switching between patterns A/B: synchronization signal is output at the top of pattern A/B. Position: 1 to {(Least common multiple of Pattern Length*1 and 64) –79}, in 16-bit steps	
	When Mixed Data is set	Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps	
	Mixed Alternate is set	Block No. setting: 1 to Block No. specified for Mixed Alternate, in single steps Mixed Alternate Content: Switching between patterns A/B Row No. setting: 1 to the Row No. specified for Mixed Alternate, in single steps	
	When Sequence is set	Block No. setting: 1 to Block No. set for Sequence Pattern, in single steps Position: 1 to {(Least common multiple of Pattern Length*1 and 64) –79}, in 16-bit steps	
	Burst Output2	Trigger Delay: 0 to Burst Cycle – 64 bits, in 16-bit steps Enable Pulse Width: 0 to Burst Cycle – 64 bits, in 16-bit steps	Can be selected when Burst is set.
	Output level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Impedance	50 Ω/GND	
	Connector	SMA	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Gating output	Timing Signal	Cycle : In the case of PRBS, Data, Zero Substitution: Least common multiple of Pattern Length and 64 In the case of 2 Ch Combination: 0 to (Least common multiple of Pattern Length*1 and 128) In the case of 4 Ch Combination: 0 to (Least common multiple of Pattern Length*1 and 256) In the case of Mixed: Row Length × Number of Rows × Number of Blocks In the case of Alternate: Pattern Length of Pattern A or B In the case of Sequence: Pattern length of the block specified in Pattern Sync of Aux Output.	Can be selected when Repeat is set.
		Pulse Width: In the case of PRBS, Data, Zero Substitution, Alternate: 0 to {(Least common multiple of Pattern Length*1 and 64) –64}, in 16-bit steps (0 to 64 bits when Pattern Length is 64 bits or less. The maximum settable number is 68, 719, 476, 672.) In the case of 2 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 128) -128}, in 32-bit steps (0 to 128 bits when Pattern Length is 128 bits or less. The maximum settable number is 137, 438, 953, 344.) In the case of 4 Ch Combination: 0 to {(Least common multiple of Pattern Length and 256) –256}, in 64-bit steps (0 to 256 bits when Pattern Length*1 is 256 bits or less. The maximum settable number is 274, 877, 906, 688) In the case of Mixed: 0 to Row length × Number of rows × Number of blocks –64, in 16-bit steps In the case of 4 Ch Combination, 0 to Row length × Number of rows × Number of blocks –256, in 64-bit steps In the case of Sequence: 0 to 64, in 16-bit steps (no block) 0 to {(Pattern length of the block specified in Pattern Sync of Aux Output) –64}, in 16-bit steps (with block)	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Gating output (continued)	Timing Signal (continued)	Delay: In the case of PRBS, Data, Zero Substitution, Alternate: 0 to {(Least common multiple of Pattern Length and 64) –64}, in 16-bit steps (0 to 64 bits when Pattern Length*1 is 79 bits or less. The maximum settable number is 4 294 967 232) In the case of 2 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 128) -128}, in 32-bit steps (0 to 128 bits when Pattern Length is 128 bits or less. The maximum settable number is 8 589 934 464) In the case of 4 Ch Combination: 0 to {(Least common multiple of Pattern Length* and 256) –256}, in 64-bit steps (0 to 256 bits when Pattern Length is 256 bits or less. The maximum settable number is 17 179 868 928) In the case of Mixed: 0 to Row length × Number of rows × Number of blocks –64, in 16-bit steps In the case of 2 Ch Combination: 0 to Row length × Number of rows × Number of blocks –128, in 32-bit steps In the case of 4 Ch Combination: 0 to Row length × Number of rows × Number of blocks –256, in 64-bit steps In the case of Sequence: 0 to {(Pattern length of the block specified in Pattern Sync of Aux Output) –64}, in 16-bit steps (with block)	Can be selected when Repeat is set.

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Gating output (continued)	Burst output	Enable Period: Internal 640 to 2 147 483 136 bits, in 128-bit steps Other than Internal 640 to 2 147 483 648 bits, in 128-bit steps In the case of 2 Ch Combination: Internal 1 280 to 4 294 966 272 bits, in 256-bit steps Other than Internal 1 280 to 4 294 967 296 bits, in 256-bit steps In the case of 4 Ch Combination: Internal 2 560 to 8 589 932 544 bits, in 512-bit steps Ext Trigger/Enable 2 560 to 8 589 934 592 bits, in 512-bit steps	Can be selected when Burst is set.
		Burst Cycle: 1 280 to 2 147 483 648 bits, in 128-bit steps In the case of 2 Ch Combination: 2 560 to 4 294 967 296 bits, in 256-bit steps In the case of 4 Ch Combination: 5 120 to 8 589 934 592 bits, in 512-bit steps	
		Delay: 0 to "Burst Cycle – 64" bits, in 16-bit steps In the case of 2 Ch Combination: 0 to "Burst Cycle –128" bits, in 32-bit steps In the case of 4 Ch Combination: 0 to "Burst Cycle –256" bits, in 64-bit steps	
		Pulse Width: 0 to "Burst Cycle – 64" bits, in 16-bit steps In the case of 2 Ch Combination 0 to "Burst Cycle –128" bits, in 32-bit steps In the case of 4 Ch Combination 0 to "Burst Cycle –256" bits, in 64-bit steps	
	Output level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Termination	50 Ω/GND	
	Connector	SMA	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Data output (Defined with PRBS2^{23} – 1, Mark Ratio 1/2)	Number of outputs	2 (Data/$\overline{\text{Data}}$ not independent)	For MU181020A-001 only
	Output amplitude	0/–0.5 V (Fixed) H: –0.20 to 0.10 V L: –0.65 to –0.40 V	
	Cross Point	50 ±15% (Fixed)	
	Rising/falling time	Typ. 30 ps (20 to 80%) (≥5 Gbit/s) Typ.40 ps(20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 15 ps (p-p)*2	
	Termination	50 Ω/GND	
	Connector	SMA	
	Number of outputs	2 (Data/$\overline{\text{Data}}$ Not independent)	For MU181020A-002 only
	Output amplitude	0/–1.0 V (Fixed) H: –0.25 to 0.05 V L: –1.4 to –0.85 V	
	Cross Point	50 ±15% (Fixed)	
	Rising/falling time	Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ. 45 ps(20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps (p-p)*2	
	Termination	50 Ω/GND	
	Connector	SMA	
Data output (MU181020A-x10) Variable Data Output (0.05 to 0.8 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020A-x10 is installed
	Output amplitude	0.05 to 0.8 Vp-p, in 2 mV steps (Not independent, variable)	
		Setting error: ±50 mV ±17% (≥0.1 Vp-p) ±25 mV ±17% (<0.1 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Setting error: ±65 mV ±10% of offset ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, NCML, PCML, LVPECL, LVDS (200 mVp-p, 400 mVp-p)	
	Tracking	Available	
	Cross Point	30 to 70%, in 1% steps (Not independent, variable)	
	Rising/falling time	Typ. 28 ps (20 to 80%) (≥5 Gbit/s, >0.2 Vp-p) Typ. 35 ps(20 to 80%) (<5 Gbit/s, >0.2 Vp-p)	
	Total Jitter	Typ. 15 ps (p-p) (when installed in MU181020A-001)*2 Typ. 10 ps (p-p) (when installed in MU181020A-002)*2	

*2: The jitter specification is the value when using an item with an oscilloscope residual jitter of less than 200 fs (rms).

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Data output (MU181020A-x10) Variable Data Output (0.05 to 0.8 Vp-p) (continued)	Waveform distortion (0 peak)	Typ. ±14% (10 Gbit/s, amplitude: 0.5 to 0.8 Vp-p)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω	
	Connector	SMA	
	Offset reference	Can be switched between Voh, Vth and Vol	
Data output (MU181020A-x11) Variable Data Output (0.25 to 2.5 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020A-x11 is installed
	Output amplitude	0.25 to 2.5 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV, ±17%	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Setting error: ±65 mV ±10% of offset ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (400 mVp-p)	
	Tracking	Available	
	Cross Point	30 to 70%, in 1% steps (Independent, variable)	
	Rising/falling time	Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 15 ps p-p (when installed in MU181020A-001)*2 Typ. 10 ps p-p (when installed in MU181020A-002)*2	
	Waveform distortion (0 peak)	Typ. 25 mV ±6% (10 Gbit/s)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Data output (MU181020A-x12) High Performance Data Output (0.05 to 2.0 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020A-x12 is installed
	Output amplitude	0.05 to 2.0 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV ±17% (≥0.1 Vp-p) ±25 mV ±17% (<0.1 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV (Independent, variable)	
		Setting error: ±65 mV ±10% of offset (Vth) ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (200 mVp-p, 400 mVp-p)	
	Tracking	Available	
	Cross Point	20 to 80%, in 1% steps (Independent, variable)	
	Rising/falling time	Typ. 20 ps (20 to 80%) (at 2 Vp-p, for 12.5 Gbit/s, 10 Gbit/s)	
		Typ. 25 ps (10 to 90%) (at 2 Vp-p, for 12.5 Gbit/s, 10 Gbit/s)	
	Total Jitter	Typ. 15 ps p-p (when installed in MU181020A-001)*2	
		Typ. 8 ps p-p (when installed in MU181020A-002)*2	
	Waveform distortion (0 peak)	Typ. ±25 mV±6% (10 Gbit/s)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC.	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)/50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	

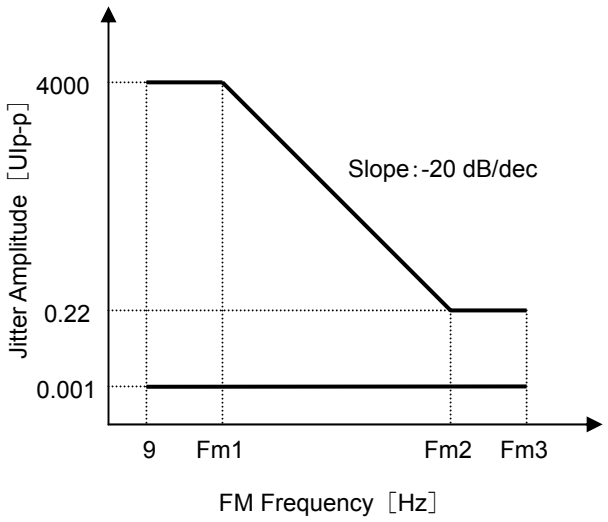
Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Data output (MU181020A-x13) Variable Data Output (0.5 to 3.5 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020A-x13 is installed
	Output amplitude	0.5 to 3.5 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV ±17%	
		Crossing point: 20 to 80% (@10 Gbit/s, Amplitude: 1.0 to 3.0 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Minimum value: −4.0 Vol	
		Setting error: ±65 mV ±10% of offset (Vth) ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL	
	Tracking	Available	
	Cross Point	20.0 to 90.0%, in 0.1% steps (Independent, variable)	
	Rising/falling time	Typ. 25 ps (20 to 80%) (at ≥1 Vp-p, for 10 Gbit/s)	
	Total Jitter	Typ. 8 ps p-p (10 Gbit/s)*2	
	Waveform distortion (0 peak)	Typ. ±25 mV±10% (10 Gbit/s, ≥2 Vp-p)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC.	
		For DC: GND, –2 V, +1.3 V, +3.3 V/50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	
Clock output	Number of outputs	1 (Clock)	
	Output amplitude	0.5 Vp-p ±0.25 V (AC) (Fixed) (at 8 to 12.5 GHz) 0.65 Vp-p ±0.25 V (AC) (Fixed) (at 0.1 to 8 GHz)	
	Duty	50 ±15% (Fixed)	
	Rising/falling time	Typ. 30 ps (20 to 80%) (at 10 GHz, 12.5 GHz)	
	Total Jitter	Typ. 2 ps (RMS) (when installed in MU181020A-001)*2	
		Typ. 1 ps (RMS) (when installed in MU181020A-002)*2	
	Termination	AC/50 Ω	
	Connector	SMA	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Clock output (MU181020A-x21) (0.1 to 2.0 Vp-p)	Number of outputs	2 (Clock/$\overline{\text{Clock}}$)	When MU181020 A-x21 is installed
	Output amplitude	0.1 to 2.0 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±70 mV ±17% (≥0.2 Vp-p) ±50 mV ±17% (<0.2 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Setting error: ±65m V ±10% of offset ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (200 mVp-p, 400 mVp-p)	
	Tracking	Available	
	Duty	–25 to +25, in single steps (No Unit) (Not independent)	
	Rising/falling time	Typ. 24 ps (20 to 80%)	
	Total Jitter	Typ. 2 ps (RMS) (when installed in MU181020A-001)*2	
		Typ. 1 ps (RMS) (when installed in MU181020A-002)*2	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	
Variable Data Delay (MU181020A-x30)	Phase variable range	–1000 to +1000 mUI, in 1 mUI steps In the case of 4 Ch Combination or Channel Synchronization: –64 000 to +64 000 mUI, in 1-mUI steps	When MU181020 A-x30 is installed
	Phase setting error	Typ. 20 mUIp-p mUI (after calibration)	
	mUI/ps switching	mUI/ps switching in 1/1 Clock frequency	
	Relative'0'	Available from the screen operation	
	Combination	Available from the screen operation	
	Phase relationship between Data and Clock	±100 mUI or less	

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter</td><td>Jitter tolerance mask</td><td>


<table>
<tr><th>Fc［GHz］</th><th>Fm1 [Hz]</th><th>Fm2 [Hz]</th><th>Fm3 [Hz]</th></tr>
<tr><td>6.4 < Fc ≤ 12.5</td><td>220</td><td>4 M</td><td>80 M</td></tr>
<tr><td>3.2 < Fc ≤ 6.4</td><td>110</td><td>2 M</td><td>40 M</td></tr>
<tr><td>1.6 < Fc ≤ 3.2</td><td>55</td><td>1 M</td><td>20 M</td></tr>
<tr><td>0.8 < Fc ≤ 1.6</td><td>27.5</td><td>500 k</td><td>10 M</td></tr>
<tr><td>0.1 ≤ Fc ≤ 0.8</td><td>13.75</td><td>250 k</td><td>5 M</td></tr>
</table>
Measurement conditions:
・ "Internal" is selected for the modulation of the MU181000A 12.5 GHz Synthesizer (with Option 001) or MU181000B 12.5 GHz 4 port Synthesizer (with Option 001) (hereinafter referred to as MU181000A/B)and the clock is input to the external clock input connector of the MU181020A.
・ Measurement pattern: PRBS $2^{31} - 1$
・ Error measurement is performed by the MU181040A.
</td><td>When MU181020A-002 is installed</td></tr>
</table>

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter</td><td>Jitter tolerance (80 MHz or higher modulation)</td><td>
<table>
<tr><th>Fc [GHz]</th><th>FM Frequency [Hz]</th><th>Jitter Amplitude [UIp-p] (Max.)</th></tr>
<tr><td rowspan="2">11.3 < Fc ≤ 12.5</td><td>250 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 250 M</td><td>0.22</td></tr>
<tr><td>8.5 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td rowspan="2">8.0 < Fc ≤ 8.5</td><td>500 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>4.0 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td>2.4 < Fc ≤ 4.0</td><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>1.4 < Fc ≤ 2.4</td><td>80 to 100 M</td><td>0.22</td></tr>
</table>
Measurement conditions:
• "External" is selected for the modulation of the MU181000A/B (with Option 001 installed), and the clock is input to the external clock input connector of the MU181020A.
In this event, Fc ≤ 1.4 GHz and Fm3 of the jitter tolerance mask above must be as follows:
<table>
<tr><th>Fc [GHz]</th><th>Fm3 [Hz]</th></tr>
<tr><td>0.65 < Fc ≤ 1.4</td><td>20 M</td></tr>
<tr><td>0.4 < Fc ≤ 0.65</td><td>10 M</td></tr>
<tr><td>0.1 ≤ Fc ≤ 0.4</td><td>5 M</td></tr>
</table>
• Use Recovered Clock at the clock recovery operation frequency (except 4.25 GHz) of Option x20. (At other frequencies, use External input clock to assure the above performance.)
• Measurement pattern: PRBS $2^{31} - 1$
• Ambient temperature: 25 ±5°C</td><td>When MU181020A-002 is installed</td></tr>
</table>

Table 1.3.1-1 Specifications for MU181020A (Cont'd)

Item		Specifications	Remarks
Unit Sync	ON/OFF*3	Available	Some restrictions on Combination Settings*3
	Unit Sync Output	Gating Output connector output Pulse Width: 64-bit Delay: Same as Timing Signal (Repeat)	
	Unit Sync Input	Input from AUX Input connector Unit Sync (generates pattern synchronized with rising edge detection) The input specifications are equal to that of Aux Input.	
	Unit Offset	–1000 to +1000 mUI, 1 mUI step At Combination, Channel Synchronization: –64 000 to +64 000 mUI, 1 mUI step However, restricted by Delay setting	
Size	Dimensions	234(W) x 21(H) x 175(D) mm (excluding Compact-PCI 1 slot and protruding parts)	
	Mass	2.5 kg max. (including options)	
Environmental performance	Operating Temperature	5° to 40°C (ambient temperature of installed equipment)	
	Storage Temperature	–20° to +60°C (recommended: 5° to 30°C)	

*3: Enabled at Independent, 4ch Combination, 25Gx2ch Combination, 12.5G Channel Synchronization, and 25G Channel Synchronization settings

1.3.2 Specifications for MU181020B

Table 1.3.2-1 Specifications for MU181020B

Item		Specifications	Remarks
Operating frequency range		0.1 to 14 GHz (When MU181040B-002 is installed) 0.1 to 14.05 GHz (When MU181040B-002 and 003 are installed) 0.1 to 14.1 GHz (When MU181040B-002 and 005 are installed)	
Pattern generation		Repeat/Burst	
Data Sequence		Restart/Consecutive/Continuous	When Burst is set
Generated pattern			
PRBS	Pattern length	2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Mark ratio	1/2, 1/4, 1/8, 0/8, 1/2INV, 3/4, 7/8, 8/8	
	Number of AND bit shifts at the mark ratio	1 bit/3 bits (at 1/4, 3/4, 7/8, 1/8)	
Zero Substitution	Pattern length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)	
	Successive-zeros bit length	1 to "pattern length – 1" bits can be inserted. When the next bit is "0" after "0" conversion, the bit is changed to "0".	
Data	Pattern length	2 to 134 217 728 bits, in 1-bit steps In the case of 2 Ch Combination: 4 to 268 435 456 bits, in 2-bit steps In the case of 4 Ch Combination: 8 to 536 870 912 bits, in 4-bit steps	
Alternate	Data Length	128 to 67 108 864 bits, in 128-bit steps Can be set independently for patterns A and B.	Cannot be set when Combination or Burst is set.
	Loop Control	Internal: Auto switching depending on A/B Loop count settings External: Controlled by external signal (H:A Pattern, L:B Pattern) Manual (1 shot asynchronous): B pattern for the number specified comes out when pressing the button.	
	Loop Time	1 to 511 times, in 1-time steps Can be set independently for patterns A and B.	
Mixed	Loop Control	Alternate switching control	
	Loop Time	1 to 511 times, in 1-time steps Can be set independently for patterns A and B.	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Mixed (continued)	Number of blocks	1 to the smallest number among a to d, below, in 1-block steps a) 511 b) INT (128 Mbits × x/(Number of rows × Data Length')) where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT(Data Length/(128 × x)) +1) × 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of blocks fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31}) × x/(Row Length × Number of rows)) where x is: 1 for Independent 2 for 2 Ch Combination 4 for 4 Ch Combination d) (Row Length – Data Length) × Number of blocks ≥ 2^31 (2 147 483 648)	
	Pattern	Data, Alternate (Alternate cannot be set for Combination.)	
	Data Length	512 to 134 217 728 bits (Data) 512 to 67 108 864 bits (Alternate) In the case of 2 Ch Combination 1 024 to 268 435 456 bits, in 2-bit steps (Data) In the case of 4 Ch Combination 2 048 to 536 870 912 bits, in 4-bit steps (Data) PRBS length: $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)	
	Row Length	768 to 2 281 701 376 bits, in 128-bit steps (Data) 768 to 2 214 592 512 bits, in 128-bit steps (Alternate) In the case of 2 Ch Combination: 1 536 to 4 563 402 752 bits, in 256-bit steps (Data) In the case of 4 Ch Combination: 3 072 to 9 126 805 504 bits, in 512-bit steps (Data)	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Mixed (continued)	Number of rows	1 to the smallest number among a to c, below, in 1-row steps a) 16 b) INT(128 Mbit × x/Data Length') where Data Length' is: - When Data Length is indivisible by (128 × x) =(INT(Data Length/(128 × x))+1)× 128 × x - When Data Length is divisible by (128 × x) =Data Length The maximum number of rows fulfilling the following formula applies: Data Length' × Number of rows × Number of blocks ≤ 128 Mbits c) INT((128 Mbits +2^{31})× x/Row Length) where x is; 1 in the case of Independent 2 in the case of 2 Ch Combination 4 in the case of 4 Ch Combination	
	PRBS steps /mark rate	Equal to PRBS	
	PRBS Sequence	Restart/Consecutive	
	Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)	
Sequence	Block number	1 to 128 /1 Step	Cannot be set when Combination or Burst is set.
	Block length	16 384 to 1 048 576 bits, in 128-bit steps	
	Loop time	1 to 1 024 times, in 1-time steps, or repeat	
	Sequence conditions	Can be set independently for each block. A pattern match, B pattern match, Manual, Trigger loop complete, External trigger	
	Next destination	Next, Stop, Jump, None	
Pattern Sequence	Repeat	Continuous Pattern	
	Burst	Burst Pattern (supports PRBS, Zero-Substitution, Data and Mixed) Source: Internal, External-Trigger (AUX Input), External-Enable (AUX Input) Data Sequence: Restart, Consecutive, Continuous Burst Cycle: 1 280 to 2 147 483 648 bits / 128 bits step Enable period: 640 to 2 147 483 520 bits / 128 bits	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Logical inversion		Can be switched between Positive and Negative.	
Error addition	Area	ALL, Specific block (Can be selected only for ALTN, Mixed and Sequence.)	
	Error source switching	Can be switched among Internal, External-Trigger and External-Disable. (Use AUX input for external input.)	
	Error Variation	Repeat, Single	
	Error Ratio	x E–n (x = 1 to 9, n = 2 to 12)	n=3 to 12 when Combination is set.
	Insertion CH	1 to 32, CH Scan (Only when Internal is set.)	
External clock input	Input frequency range	0.1 to 14 GHz (When MU181040B-002 is installed) 0.1 to 14.05 GHz (When MU181040B-002 and 003 are installed) 0.1 to 14.1 GHz (When MU181040B-002 and 005 are installed)	
	Input amplitude	0.4 to 1.5 Vp-p (–4 to 7.5 dBm)	
	Input waveform	100 to 500 MHz: Rectangular wave	
		> 500 MHz: Sine wave or rectangular wave (Duty: 50%)	
	Termination	AC/50 Ω	
	Connector	SMA	
AUX input	Input signal selection	Alternate Control (L: pattern A, H: pattern B) When Alternate or Mixed-Alternate is selected as the generated pattern.	
		Sequence Control (transits to the next sequence at rising edge detection) When Sequence is selected as the generated pattern.	
		Error Injection (error occurs at rising edge detection) In the case of 2 or 4 Ch Combination, input only to Master Module is enabled.	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
AUX input (continued)	Input signal selection (continued)	Burst: When Burst is set in Pattern Sequence, and Source is set to other than Internal. In the case of 2 or 4 Ch Combination: input only to Master Module is enabled. External Trigger (data occurs at rising edge detection) External Enable (L: Data disable, H: Data enable)	
	Minimum pulse width	1/64 of data rate	
	Input level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Termination	50 Ω/GND	
	Connector	SMA	
AUX output	Output signal selection	1/N Clock Pattern Sync/Burst Output2 Burst Output2 is enabled when Burst is set in Pattern Sequence.	
	1/N Clock	1/N: N = 2, 4, 8, 9, 10…510, 511	
	Pattern Sync		
	When PRBS, Data or Zero-substitution is set	Position: 1 to {(Least common multiple of Pattern Length*1 and 64) –79}, in 16-bit steps The maximum settable number is 68 719 476 657 In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length*1 and 128) –159}, in 32-bit steps The maximum settable number is 137 438 953 313. In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length*1 and 256) –319}, in 64-bit steps The maximum settable number is 274 877 906 625.	
	When Alternate is set	Switching between patterns A/B: synchronization signal is output at the top of pattern A/B.	
		Position: 1 to {(Least common multiple of Pattern Length*1 and 64) –79}, in 16-bit steps	

*1: At Independent, when the pattern length is 127 bits or less, specify the length as an integer multiple so that it becomes 128 bits or more.
At 2 Ch Combination, when the pattern length is 255 bits or less, specify the length as an integer multiple so that it becomes 256 bits or more.
At 4 Ch Combination, when the pattern length is 511 bits or less, specify the length as an integer multiple so that it becomes 512 bits or more.

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
AUX output (continued)	When Mixed Data is set	Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps	
		Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps	
	Mixed Alternate is set	Block No. setting: 1 to Block No. specified for Mixed Alternate, in single steps	
		Mixed Alternate Content: Switching between patterns A/B	
		Row No. setting: 1 to the Row No. specified for Mixed Alternate, in single steps	
	When Sequence is set	Block No. setting: 1 to Block No. set for Sequence Pattern, in single steps	
		Position: 1 to {(Least common multiple of Pattern Length*1 and 64) -79}, in 16-bit steps	
	Burst Output2	Trigger Delay: 0 to Burst Cycle – 64 bits, in 16-bit steps	Can be selected when Burst is set.
		Enable Pulse Width: 0 to Burst Cycle – 64 bits, in 16-bit steps	
	Output level	0/–1 V H: –0.25 to 0.05 V L: –1.25 to –0.80 V	
	Impedance	50 Ω/GND	
	Connector	SMA	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Gating output	Timing Signal	Cycle : In the case of PRBS, Data, Zero Substitution: Least common multiple of Pattern Length and 64 In the case of 2 Ch Combination: 0 to (Least common multiple of Pattern Length*1 and 128) In the case of 4 Ch Combination: 0 to (Least common multiple of Pattern Length*1 and 256) In the case of Mixed Row Length × Number of Rows × Number of Blocks In the case of Alternate Pattern Length of Pattern A or B In the case of Sequence Pattern length of the block specified in Pattern Sync of Aux Output.	Can be selected when Repeat is set.
		Pulse Width: In the case of PRBS, Data, Zero Substitution, Alternate: 0 to {(Least common multiple of Pattern Length*1 and 64) –64}, in 16-bit steps (0 to 64 bits when Pattern Length is 64 bits or less. The maximum settable number is 68 719 476 672.) In the case of 2 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 128) –128}, in 32-bit steps (0 to 128 bits when Pattern Length is 128 bits or less. The maximum settable number is 137 438 953 344.) In the case of 4 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 256) –256}, in 64-bit steps (0 to 256 bits when Pattern Length is 256 bits or less. The maximum settable number is 274 877 906 688.)	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Gating output (continued)	Timing Signal (continued)	In the case of Mixed: 0 to Row length × Number of rows × Number of blocks –64, in 16-bit steps In the case of 2 Ch Combination: 0 to Row length × Number of rows × Number of blocks –128, in 32-bit steps In the case of 4 Ch Combination: 0 to Row length × Number of rows × Number of blocks –256, in 64-bit steps In the case of Sequence: 0 to 64, in 16-bit steps (no block) 0 to {(Pattern length of the block specified in Pattern Sync of Aux Output) –64}, in 16-bit steps (with block)	Can be selected when Repeat is set.
		Delay: In the case of PRBS, Data, Zero Substitution, Alternate: 0 to {(Least common multiple of Pattern Length and 64) –64}, in 16-bit steps (0 to 64 bits when Pattern Length*1 is 79 bits or less. The maximum settable number is 4 294 967 232) In the case of 2 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 128) –128}, in 32-bit steps (0 to 128 bits when Pattern Length is 128 bits or less. The maximum settable number is 8 589 934 464) In the case of 4 Ch Combination: 0 to {(Least common multiple of Pattern Length*1 and 256) –256}, in 64-bit steps (0 to 256 bits when Pattern Length is 256 bits or less. The maximum settable number is 17 179 868 928) In the case of Mixed: 0 to Row length × Number of rows × Number of blocks –64, in 16-bit steps In the case of 2 Ch Combination: 0 to Row length × Number of rows × Number of blocks –128, in 32-bit steps In the case of 4 Ch Combination: 0 to Row length × Number of rows × Number of blocks –256, in 64-bit steps In the case of Sequence: 0 to {(Pattern length of the block specified in Pattern Sync of Aux Output) –64}, in 16-bit steps (with block)	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Gating output (continued)	Burst output	Enable Period: Internal 640 to 2 147 483 136 bits, in 128-bit steps Other than Internal 640 to 2 147 483 648 bits, in 128-bit steps In the case of 2 Ch Combination: Internal 1 280 to 4 294 966 272 bits, in 256-bit steps Other than Internal 1 280 to 4 294 967 296 bits, in 256-bit steps In the case of 4 Ch Combination: Internal 2 560 to 8 589 932 544 bits, in 512-bit steps Other than Internal 2 560 to 8 589 934 592 bits, in 512-bit steps	Can be selected when Burst is set.
		Burst Cycle: 1 280 to 2 147 483 648 bits, in 128-bit steps In the case of 2 Ch Combination: 2 560 to 4 294 967 296 bits, in 256-bit steps In the case of 4 Ch Combination: 5 120 to 8 589 934 592 bits, in 512-bit steps	
		Delay: 0 to "Burst Cycle – 64" bits, in 16-bit steps In the case of 2 Ch Combination: 0 to Burst Cycle –128 bits, in 32-bit steps In the case of 4 Ch Combination: 0 to Burst Cycle –256 bits, in 64-bit steps	
		Pulse Width: 0 to "Burst Cycle – 64" bits, in 16-bit steps In the case of 2 Ch Combination 0 to Burst Cycle –128 bits, in 32-bit steps In the case of 4 Ch Combination 0 to Burst Cycle –256 bits, in 64-bit steps	
	Output level	0/–1 V H: –0.25 to 0.05 V L: –1.10 to –0.80 V	
	Impedance	50 Ω/GND	
	Connector	SMA	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Data output (Defined with PRBS2^{23} – 1, Mark Ratio 1/2)	Number of outputs	2 (Data/$\overline{\text{Data}}$ not independent)	For MU181020 B-002 only
	Output amplitude	0/–1.0 V (Fixed) H: –0.25 to 0.05 V L: –1.4 to –0.85 V	
	Cross Point	50 ±15% (Fixed)	
	Rising/falling time	Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ.45 ps(20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps (p-p)*2	
	Termination	50 Ω/GND	
	Connector	SMA	
Data output (MU181020B-x11) Variable Data Output (0.25 to 2.5 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020 B-x11 is installed
	Output amplitude	0.25 to 2.5 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV, ±17%	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Setting error: ±65 mV ±10% of offset ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (400 mVp-p)	
	Tracking	Available	
	Cross Point	30 to 70%, in 1% steps (Independent, variable)	
	Rising/falling time	Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps (p-p)*2	
	Waveform distortion (0 peak)	Typ. 25 mV ±6% (10 Gbit/s)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	

*2: The jitter specification is the value when using an item with an oscilloscope residual jitter of less than 200 fs (rms).

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Data output (MU181020B-x12) High Performance Data Output (0.05 to 2.0 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020 B-x12 is installed
	Output amplitude	0.05 to 2.0 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV ±17% (≥0.1 Vp-p) ±25 mV ±17% (<0.1 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV (Independent, variable)	
		Setting error: ±65 mV ±10% of offset (Vth) ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (200 mVp-p, 400 mVp-p)	
	Tracking	Available	
	Cross Point	20 to 80%, in 1% steps (Independent, variable)	
	Rising/falling time	Typ. 20 ps (20 to 80%) (at 2 Vp-p, for 10 Gbit/s, 12.5 Gbit/s, 14 Gbit/s, 14.05Gbit/s*3 and 14.1 Gbit/s*4)	
		Typ. 25 ps (10 to 90%) (at 2 Vp-p, for 10 Gbit/s, 12.5 Gbit/s, 14 Gbit/s, 14.05Gbit/s*3 and 14.1 Gbit/s*4)	
	Total Jitter	Typ. 8 ps (p-p) *2	
	Waveform distortion (0 peak)	Typ. ±25 mV±6% (10 Gbit/s)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC.	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) / 50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	

*3: When MU181020B-003 is installed.

*4: When MU181020B-005 is installed.

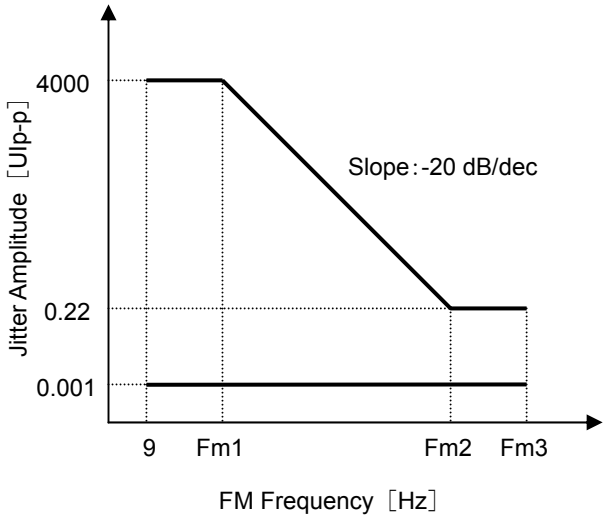
Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Data output (MU181020B-x13) Variable Data Output (0.5 to 3.5 Vp-p)	Number of outputs	2 (Data/$\overline{\text{Data}}$)	When MU181020 B-x13 is installed
	Output amplitude	0.5 to 3.5 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±50 mV ±17%	
		Crossing point: 20 to 80% (@10 Gbit/s, Amplitude: 1.0 to 3.0 Vp-p)	
		Setting error : ±50 mV ±17%	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Minimum value: −4.0 Vol	
		Setting error : ±65 mV ±10% of offset (Vth) ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL	
	Tracking	Available	
	Cross Point	20.0 to 90.0%, in 0.1% steps (Independent, variable)	
	Rising/falling time	Typ. 25 ps (20 to 80%) (at ≥1 Vp-p, for 10 Gbit/s)	
	Total Jitter	Typ. 8 ps (p-p) (10 Gbit/s, 14.05 Gbit/s*3, 14.1 Gbit/s*4)*2	
	Waveform distortion (0 peak)	Typ. ±25 mV±10% (10 Gbit/s, ≥2 Vp-p)	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC.	
		For DC: GND, –2 V, +1.3 V, +3.3 V/50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	
Clock output	Number of outputs	1 (Clock)	
	Output amplitude	0.25 to 0.9 Vp-p (AC) (Fixed) (at 8 to 14 GHz, 8 to 14.05GHz*3 and 8 to 14.1 GHz*4) 0.4 to 0.9 Vp-p (AC) (Fixed) (at 0.1 to 8 GHz)	
	Duty	50 ±15% (Fixed)	
	Rising/falling time	Typ. 30 ps (20 to 80%) (at 10 GHz, 12.5 GHz, 14 GHz, 14.05GHz*3 and 14.1 GHz*4)	
	Total Jitter	Typ. 1 ps (RMS)*2	
	Termination	AC/50 Ω	
	Connector	SMA	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Clock output (MU181020B-x21) (0.1 to 2.0 Vp-p)	Number of outputs	2 (Clock/XClock)	When MU181020 B-x21 is installed
	Output amplitude	0.1 to 2.0 Vp-p, in 2 mV steps (Independent, variable)	
		Setting error: ±70 mV ±17% (≥0.2 Vp-p) ±50 mV ±17% (<0.2 Vp-p)	
	Offset	–2.0 to +3.3 Voh, in 1 mV steps (Independent, variable)	
		Setting error: ±65m V ±10% of offset ±(Amplitude setting error/2)	
		Current limitation (Sourcing 50 mA, Sinking 80 mA)	
	Defined Interface	NECL, SCFL, NCML, PCML, LVPECL, LVDS (200 mVp-p, 400 mVp-p)	
	Tracking	Available	
	Duty	–25 to +25, in single steps (No Unit) (Not independent)	
	Rising/falling time	Typ. 24 ps (20 to 80%)	
	Total Jitter	Typ. 1 ps (RMS)*2	
	Output ON/OFF	ON/OFF function available	
	Termination	Can be switched between AC and DC	
		For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS) /50 Ω	
	Connector	K	
	Offset reference	Can be switched between Voh, Vth and Vol	
Variable Data Delay (MU181020B-x30)	Phase variable range	–1000 to +1000 mUI, in 1 mUI steps In the case of 4 Ch Combination or Channel Synchronization: –64 000 to +64 000 mUI, in 1 mUI steps	When MU181020 B-x30 is installed
	Phase setting error	Typ. 20 mUIp-p (after calibration) (at 0.1 to 14 GHz, 0.1 to 14.05GHz*3 and 0.1 to 14.1 GHz*4)	
	mUI/ps switching	mUI/ps switching in 1/1 Clock frequency	
	Relative'0'	Available from the screen operation	
	Combination	Available from the screen operation	
	Phase relationship between Data and Clock	±100 mUI or less 0.1 to 14GHz	

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter</td><td>Jitter tolerance mask</td><td>


<table>
<tr><th>Fc［GHz］</th><th>Fm1 [Hz]</th><th>Fm2 [Hz]</th><th>Fm3 [Hz]</th></tr>
<tr><td>6.4 < Fc ≤ 14*</td><td>220</td><td>4 M</td><td>80 M</td></tr>
<tr><td>3.2 < Fc ≤ 6.4</td><td>110</td><td>2 M</td><td>40 M</td></tr>
<tr><td>1.6 < Fc ≤ 3.2</td><td>55</td><td>1 M</td><td>20 M</td></tr>
<tr><td>0.8 < Fc ≤ 1.6</td><td>27.5</td><td>500 k</td><td>10 M</td></tr>
<tr><td>0.1 ≤ Fc ≤ 0.8</td><td>13.75</td><td>250 k</td><td>5 M</td></tr>
</table>
*: When installing the MU181020B-003, the upper frequency limit is 14.05 GHz can be used.
When installing the MU181020B-005, the upper frequency limit is 14.1 GHz can be used.

Measurement conditions:
• "Internal" is selected for the modulation of the MU181000A 12.5 GHz Synthesizer (with Option 001) or MU181000B 12.5 GHz 4 port Synthesizer (with Option 001) (hereinafter referred to as MU181000A/B)and the clock is input to the external clock input connector of the MU181020A.
• Measurement pattern: PRBS $2^{31} - 1$
• Error measurement is performed by the MU181040B.
</td><td>When MU181020 B-002 is installed</td></tr>
</table>

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th>Remarks</th></tr>
<tr><td>Jitter</td><td>Jitter tolerance (80 MHz or higher modulation)</td><td>
<table>
<tr><th>Fc [GHz]</th><th>FM Frequency [Hz]</th><th>Jitter Amplitude [UIp-p] (Max.)</th></tr>
<tr><td rowspan="2">11.3 < Fc ≤ 12.5</td><td>250 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 250 M</td><td>0.22</td></tr>
<tr><td>8.5 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td rowspan="2">8.0 < Fc ≤ 8.5</td><td>500 M to 1 G</td><td>0.1</td></tr>
<tr><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>4.0 < Fc ≤ 11.3</td><td>80 M to 1 G</td><td>0.22</td></tr>
<tr><td>2.4 < Fc ≤ 4.0</td><td>80 to 500 M</td><td>0.22</td></tr>
<tr><td>1.4 < Fc ≤ 2.4</td><td>80 to 100 M</td><td>0.22</td></tr>
</table>
Measurement conditions:
• "External" is selected for the modulation of the MU181000A/B (with Option 001 installed), and the clock is input to the external clock input connector of the MU181020A. In this event, Fc ≤ 1.4 GHz and Fm3 of the jitter tolerance mask above must be as follows:
<table>
<tr><th>Fc [GHz]</th><th>Fm3 [Hz]</th></tr>
<tr><td>0.65 < Fc ≤ 1.4</td><td>20 M</td></tr>
<tr><td>0.4 < Fc ≤ 0.65</td><td>10 M</td></tr>
<tr><td>0.1 ≤ Fc ≤ 0.4</td><td>5 M</td></tr>
</table>
• Use Recovered Clock at the clock recovery operation frequency (except 4.25 GHz) of Option x20. (At other frequencies, use External input clock to assure the above performance.)
• Measurement pattern: PRBS $2^{31} - 1$
• Ambient temperature: 25 ±5°C
</td><td>When MU181020B-002 is installed</td></tr>
</table>

Table 1.3.2-1 Specifications for MU181020B (Cont'd)

Item		Specifications	Remarks
Unit Sync	ON/OFF	Available	Some restrictions on Combination Settings*5
	Unit Sync Output	Gating Output connector output Pulse Width: 64-bit Delay: Same as Timing Signal (Repeat)	
	Unit Sync Input	Input from AUX Input connector Unit Sync (generates pattern synchronized with rising edge detection)	
	Unit Offset	–1000 to +1000 mUI, 1 mUI step At Combination, Channel Synchronization: –64 000 to +64 000 mUI, 1 mUI step However, restricted by Delay setting	
Size	Dimensions	234(W) x 21(H) x 175(D) mm (excluding Compact-PCI 1 slot and protruding parts)	
	Mass	2.5 kg max. (including options)	
Environmental performance	Operating Temperature	+15° to +35°C (ambient temperature of installed equipment)	
	Storage Temperature	–20° to +60°C (recommended: +5° to +30°C)	

*5: Enabled at Independent, 4ch Combination, 25Gx2ch Combination, 12.5G Channel Synchronization, and 25G Channel Synchronization settings

Chapter 2 Preparation before Use

This chapter describes preparations required before using the MU181020A.

2.1 Installation to Signal Quality Analyzer

For information on how to install the MU181020A to the Signal Quality Analyzer and how to turn on the power, refer to Chapter 2 “Preparation before Use” in the Signal Quality Analyzer Series Installation Guide.

2.2 How to Operate Application

The modules connected to the Signal Quality Analyzer are controlled by operating the MX180000A Signal Quality Analyzer Control Software (hereinafter, referred to as “MX180000A”).

For information on how to start up, shut down, and operate the MX180000A, refer to the *MX180000A Signal Quality Analyzer Control Software Operation Manual*.

2.3 Preventing Damage

Be sure to observe the rating ranges when connecting input and output of the MU181020A. Otherwise, the MU181020A may be damaged.

⚠ CAUTION

- **When signals are input to the MU181020A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **When output is used at the 50 W/GND terminator, never feed any current or input signals to the output.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **Never open the MU181020A. If you open it and MU181020A has failed or sufficient performance cannot be obtained, we may decline to repair the MU181020A.**
- **The MU181020A incorporates important parts and circuits, such as a hybrid IC, which are vulnerable to static electricity. Do not open the MU181020A to touch such components.**
- **The hybrid IC incorporated in the MU181020A is hermetically shielded. Do not open the hybrid IC. If you open it and sufficient performance cannot be obtained, we may decline to repair the MU181020A.**

⚠ CAUTION

- **To protect the MU181020A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Connect the ground connection end of the wrist strap to the conductive sheet or to the ground terminal of the mainframe.**

- **When connecting an external device such as a Bias-T to the output connectors of this equipment (PPG or MUX), if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits. Note the following precautions when using this equipment:**
  - **Do not connect or disconnect any external devices while DC voltage is impressed.**
  - **Only switch DC power sources ON and OFF when all equipment connections have been completed.**

  <Recommended procedure>
  Measurement Preparation 1:
  1. Connect all equipment.
  2. Set the DC power supply output to ON.
  3. Set the equipment output to ON and complete measurement.

  Measurement Preparation 2:
  1. Set the equipment output to OFF.
  2. Set the DC power supply output to OFF.
  3. Disconnect the equipment, or change the DUT connections.

  Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the equipment output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.

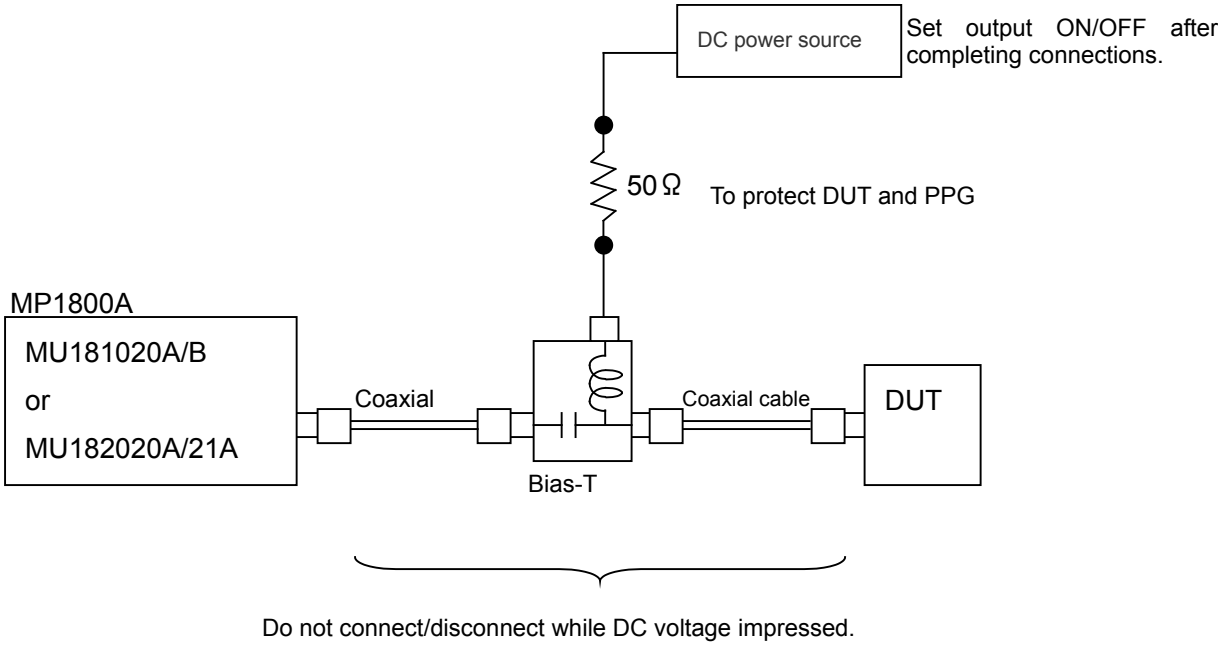


Figure 2.3-1 Bias-T Connection Example

Chapter 3 Panel Layout and Connectors

This chapter describes the panel and connectors of the MU181020A.

3.1 Panel Layout

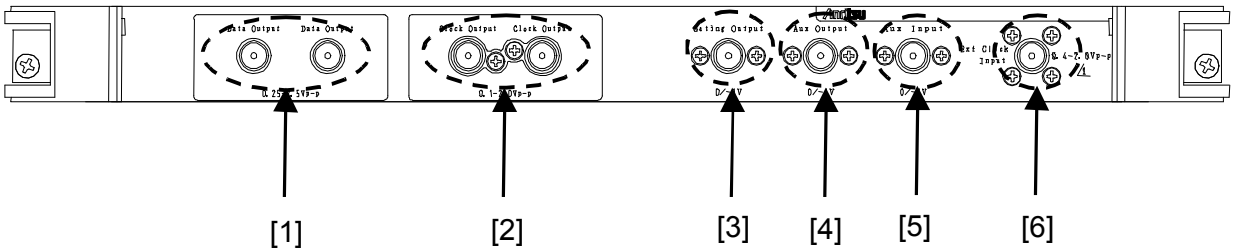


Figure 3.1-1 Panel layout

Table 3.1-1 Connectors on MU181020A panel

No.	Name	Description
[1]	Data and XData Output connectors	Outputs the differential data signals. Various interface signals can be output, depending on the installed option(s).
[2]	Clock and XClock Output connectors	Outputs the differential clock signals. Fixed to single-end output when no option is installed.
[3]	Gating Output connector	In case of Repeat: Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[4]	Aux Output connector	Outputs auxiliary signals. 1/N clock, Pattern Sync, and Burst2 can be output according to the setting.
[5]	Aux Input connector	Inputs auxiliary signals. Alternate Trigger, Sequence Trigger, Error Injection, and Burst can be selected.
[6]	Ext. Clock Input connector	Connector for MU181000A 12.5 GHz Synthesizer or for inputting Clock signal from external synthesizer.*

* We recommend using the MG3690C series as an external synthesizer. (When using a synthesizer with sine-wave output, the lower frequency limit is 500 MHz.) For details about the MG3690C series, contact Anritsu or our sales representative.

3.2 Inter-Module Connection

A connection example between the MU181020A, MU181000A 12.5 GHz Synthesizer (hereinafter, referred to as "MU181000A"), and MU181040A 12.5 Gbit/s Error Detector (hereinafter, referred to as "MU181040A") that are installed into a mainframe is shown below. Use the following procedure to connect these devices.

Note:

Avoid static electricity when handling the devices.

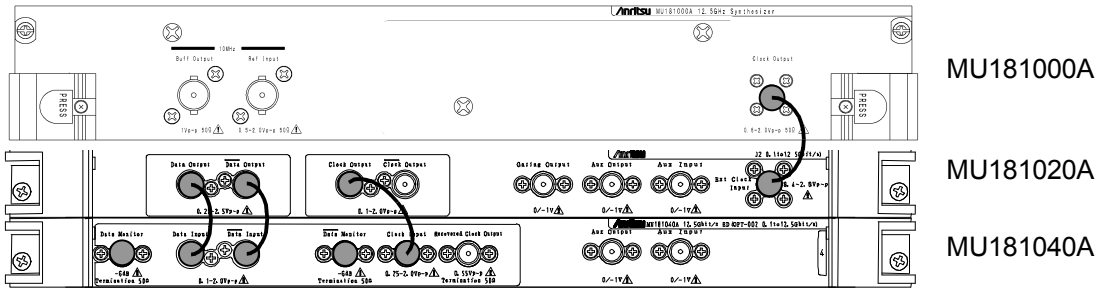


Figure 3.2-1 Inter-module connection example

1. Connect the 3-pin power cord of the mainframe to the power receptacle. Be sure to use the 3-pin power cord supplied with the mainframe and a 3-pin receptacle.
2. Connect the Clock Output connector of the MU181000A and the Ext. Clock Input connector of the MU181020A, using a coaxial cable.
3. Connect the Data Output connector of the MU181020A and the Data Input connector of the MU181040A, using a coaxial cable. Also connect the XData Output connector of the MU181020A and the XData Input connector of the MU181040A, using a coaxial cable.
4. Connect the Clock Output connector of the MU181020A and the Clock Input connector of the MU181040A, using a coaxial cable.
5. Select "Initialize" from the File menu on the menu bar to initialize the entire system. Note that all of the settings are returned to the initial settings at factory shipment after initialization. Save the settings before initialization, if necessary, by selecting "Save" from the File menu.

⚠ WARNING

- **When signals are input to this MU181020A, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **The power supply voltage rating for the mainframe is shown on the rear panel. Be sure to operate the mainframe within the rated voltage range. The mainframe may be damaged if a voltage out of the rating range is applied.**
- **To protect the MU181020A from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Connect the ground connection end of the wrist strap to the conductive sheet or to the ground terminal of the mainframe.**
- **When removing a cable from a connector on the front panel of the MU181020A, be careful not to add excessive stress to the connector. Addition of excessive stress to a connector may result in characteristic degradation or a failure.**
  Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.
- **The ALL0s pattern is set when the data output option is not installed and output is set to OFF.**
- **ON/OFF cannot be set when the clock output option is not installed.**

Chapter 4 Configuration of Setup Dialog Box

This chapter describes the configuration of the MU181020A setup dialog box.

4.1 Configuration of Entire Setup Dialog Box

The configuration of the setup dialog box when the MU181020A is inserted into a mainframe is shown below.

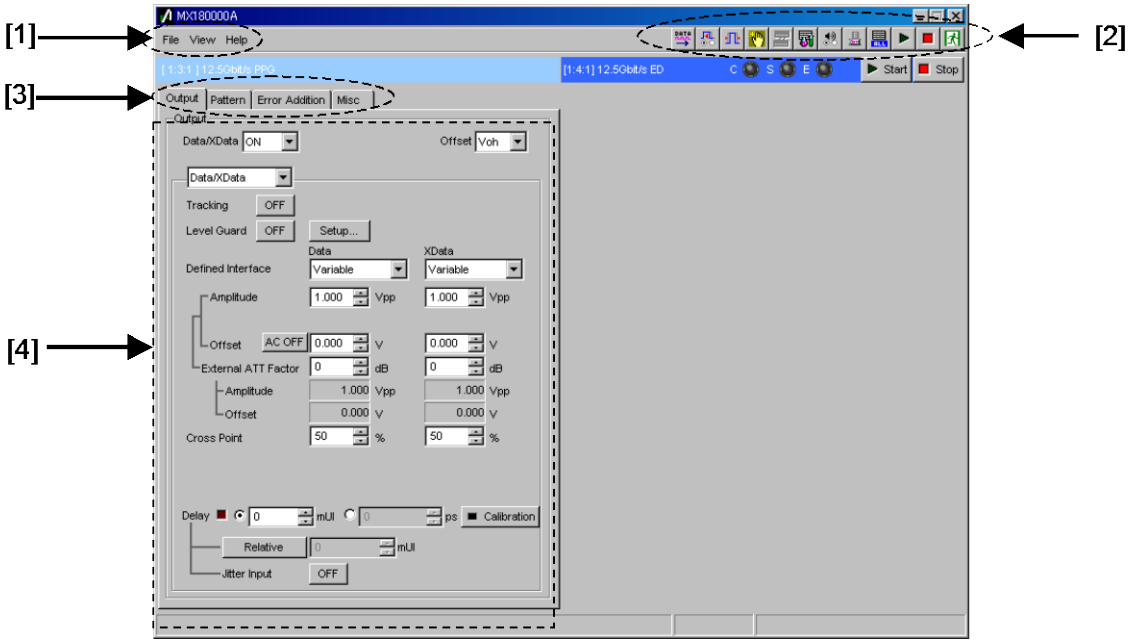


Figure 4.1-1 Configuration of entire setup dialog box for MU181020A

The setup dialog box mainly consists of four blocks ([1] to [4] in the figure above). The following table describes each of the blocks.

Table 4.1-1 Functions of blocks

No.	Block	Function
[1]	Menu bar	Selects the setting functions related to the entire device.
[2]	Module function buttons	Shortcut buttons for the function items specific to the displayed module. Users can customize up to 17 pre-defined function buttons according to their own applications.
[3]	Function setting selection tabs	Click to switch the module operation tab window according to the function items. See Chapter 5 “Operation Method” for details.
[4]	Operation tab window	Configures settings specific to each module. See Chapter 5 “Operation Method” for details.

4.2 Operation Tab Windows

The MU181020A operation tab windows are listed below. See Chapter 5 "Operation Method" for details on each operation tab window.

Figure 4.2-1 Function setting selection tabs

Table 4.2-1 Function setting selection tabs

Tab name	Functions
Output	Selection and setting of Data/XData and Clock/XClock outputs Various output interface settings can be configured in this tab window.
Pattern	Selection and setting of test pattern A test pattern can be selected and edited in this tab window.
Error Addition	Selection and setting of error addition The error addition function can be set in this tab window.
Misc	Other settings Pattern generation method setting, auxiliary input/output selection, and other settings can be configured in this tab window.

Chapter 5 Operation Method

This chapter describes the functions provided in the function setting selection tabs on the MU181020A operation window.

5.1 Setting Output Interface

Click the Output tab on the operation tab window to open the Output tab window. The output interface can be set in this window.

In the Output tab window, the settings for the Data, XData, Clock, and XClock can be configured. In addition, the CMU Bit-rate can be set when MU181020A-001 is installed.

The Data signal is output from the Data connector of the MU181020A, and the XData signal is output from the Data connector. Also, the Clock signal is output from the Clock connector, and the XClock signal is output from XClock connector. Hereinafter, the settings for the Data and XClock connectors are described as the settings for XData and XClock, respectively.

5.1.1 Setting Data/XData

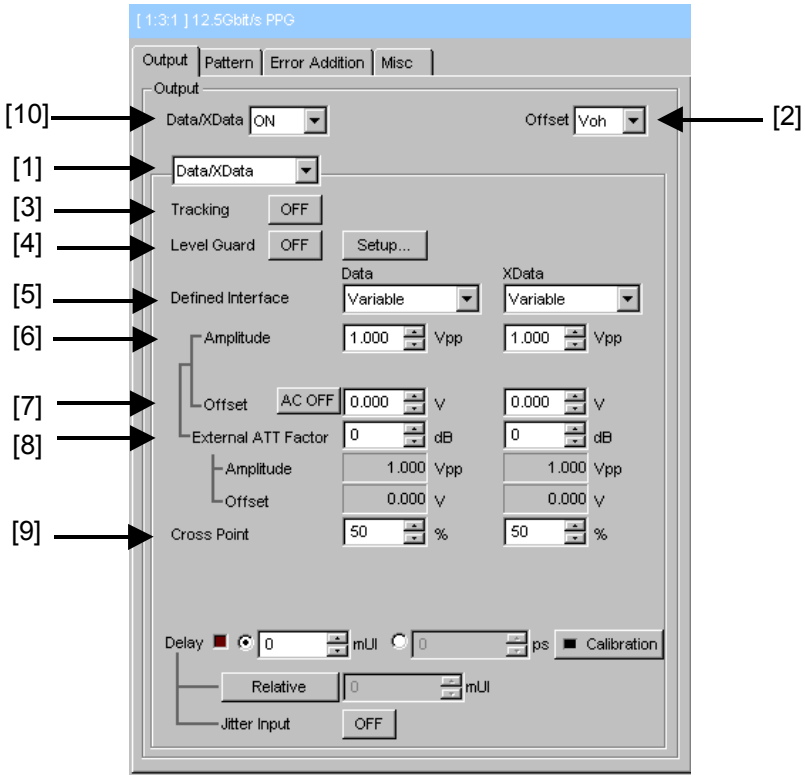


Figure 5.1.1-1 Output tab window for setting Data/XData

[1] Select “Data” or “XData” from the list box.

[2] Select the offset reference from the list box. The setting range for the offset and amplitude is restricted by each setting value. Refer to Appendix A "Pseudo-Random Pattern (PRBS Pattern)" and Appendix C "Setting Restrictions" for details on the setting ranges for the offset and amplitude. When the offset reference is changed, the offset value is calculated and changed based on the changed offset reference.

Table 5.1.1-1 Offset reference

Offset reference	Description
Voh	The offset value is set based on the high level.
Vth	The offset value is set based on the center level between the high and low levels.
Vol	The offset value is set based on the low level.

Note:

Only Voh is available when neither MU181020A-x10, -x11, -x12, -x13 -x21, MU181020B-x11, -x12, -x13 nor -x21 is installed.

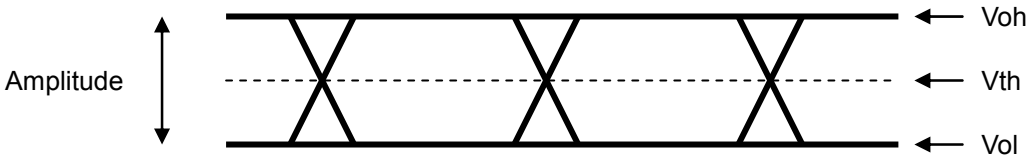


Figure 5.1.1-2 Setting data offset

[3] Set Tracking ON/OFF. When Tracking is set to ON, the settings for the XData become the same as those for the Data. This setting is valid when any of MU181020A-x10, -x11, -x12, -x13, MU181020B-x11, -x12, or -x13is installed.

[4] Configure the level guard settings. Click [Setup] to open the setup dialog box, and set the maximum amplitude (Amplitude), maximum offset (Offset Max (Voh); maximum value of the offset high level), and minimum offset (Offset Min (Vol); minimum value of the offset low level) for level guard, so that an excessively high voltage is not applied to the DUT.
This setting is valid when any of MU181020A-x10, -x11, -x12, -x13, MU181020B-x11, -x12, or -x13 is installed.
When the external ATT factor is set (refer to [8] below), the level guard settings (Amplitude, Offset Max (Voh), and Offset Min (Vol)) after passing through the fixed attenuator, which is connected between the MU181020A and the DUT, limit the output level of these setting value. Therefore, if you use the fixed attenuator without connecting, a signal exceeding the setting value is output.

[5] Separately configure the defined interface setting for Data and XData.
Note that it may not be possible to select some items, depending on the level guard setting.
This setting is valid when any of MU181020A-x10, -x11, -x12, -x13, MU181020B-x11, -x12, or -x13 is installed. When MU181020A-x10 is installed, the setting for XData becomes invalid, and the setting for Data will be applied.

Table 5.1.1-2 Amplitude setting values

Item	Amplitude		Offset Vth	Options
	Voh	Vol		
Variable	–	–	–	x10/x11/x12/x13
PCML	+3.3 V	+2.8 V	+3.05 V	x10/x11/x12/x13
NCML	0.0 V	–0.5 V	–0.25 V	x10/x11/x12/x13
SCFL	0.0 V	–0.9 V	–0.45 V	x11/x12/x13
NECL	–0.9 V	–1.7 V	–1.3 V	x10/x11/x12/x13
LVPECL	+2.4 V	+1.6 V	+2.0 V	x10/x11/x12/x13
LVDS (200 mV)	+1.3 V	+1.1 V	+1.2 V	x10/x12
LVDS (400 mV)	+1.4 V	+1.0 V	+1.2 V	x10/x11/x12

Note:

Options x10 is supported only by the MU181020A.

[6] Separately set the amplitude for Data and XData.
The setting range varies depending on the level guard setting, offset setting, and installed option.
The amplitude setting ranges when Defined Interface is set to Variable are shown in the table below. When MU181020A-x10 is installed, the setting for XData becomes invalid, and the setting for Data will be applied.

Table 5.1.1-3 Amplitude setting range

Installed Option	Amplitude setting range	Resolution
001 only	Fixed to 0.5 Vp-p	–
002 only	Fixed to 1.0 Vp-p	–
003	Fixed to 1.0 Vp-p	–
x10	0.05 to 0.8 Vp-p	0.002 V
x11	0.25 to 2.5 Vp-p	0.002 V
x12	0.05 to 2 Vp-p	0.002 V
x13	0.5 to 3.5 Vp-p	0.002 V

Note:

Options 001 and x10 are supported only by the MU181020A.
Option 003 is supported only by the MU181020B.

[7] Separately set the offset for Data and XData.
The setting range varies depending on the level guard setting, amplitude setting, and installed option.
The offset setting ranges when Defined Interface is set to Variable are shown in the table below.
Clicking to change [AC OFF] to [AC ON] enables AC-coupled output.
The lower-band cutoff frequency is about 10 kHz.

Table 5.1.1-4 Offset setting range

Installed Option	Offset setting range	Resolution	AC output
001 only	Fixed to 0.000 V (Offset: Voh)	–	Invalid
002 /003 only	Fixed to 0.000 V (Offset: Voh)	–	Invalid
x10	–3.0 to 3.3 V	0.001 V	Valid
x11	–4.5 to 3.3 V	0.001 V	Valid
x12	–4.0 to 3.3 V	0.001 V	Valid
x13	–4.0 to 3.3 V	0.001 V	Valid

Note:

Options 001 and x10 are supported only by the MU181020A.
Option 003 is supported only by the MU181020B.

[8] Separately set the external ATT factor for Data and XData. When a fixed attenuator is connected to the Data/XData output connector of the MU181020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to Variable, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicates the amplitude and offset value after passing through the attenuator, respectively.

[9] Separately set the cross point setting for Data and XData. The setting range varies depending on the installed option. This setting is valid when any of MU181020A-x10, -x11, -x12, -x13, MU181020B-x11, -x12, -x13 or -x21 is installed.

Table 5.1.1-5 Cross point setting range

Installed Option	Data/XData independency	Cross point setting range	Resolution
001 only	–	50%	–
002/003 only	–	50%	–
x10	The setting for XData is determined in conjunction with the setting for Data.	Data: 30 to 70% XData: 70 to 30%	1%
x11	Independent	30 to 70%	1%
x12	Independent	20 to 80%	1%
x13	Independent	20.0 to 90.0%	0.1%

Note:

Options 001 and x10 are supported only by the MU181020A.
Option 003 is supported only by the MU181020B.

[10] Set Output ON/OFF.

This setting applies to the selected MU181020A. When enabling the output signal (ON), enabling the output of all the instruments, by clicking the Output module function button on the menu bar, is also required. The ALL1s pattern is set when the data output option (MU181020A-x10, -x11, -x12, -x13, MU181020B-x11, -x12, or -x13) is not installed and output is set to OFF.

Notes:

- The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.
- When PCML, LVPECL, or ECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU181020A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.
- Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially-available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.
- The current for the output part is limited (50 mA for sourcing current and 80 mA for sinking current) for protection. If an overcurrent flows due to the wrong interface condition, the offset voltage for an observed waveform may therefore not reach the set level.

- Be sure to confirm that a fixed attenuator is connected between the MU181020A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

5.1.2 Setting delay

With this equipment, the Data output phase can be varied relative to the Clock output when either the MU181020A-x30 or MU181020B-x30 is installed.

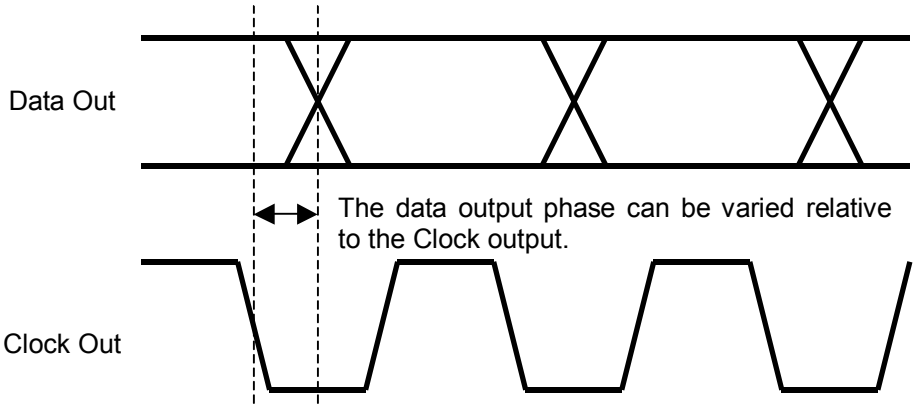


Figure 5.1.2-1 Delay setting

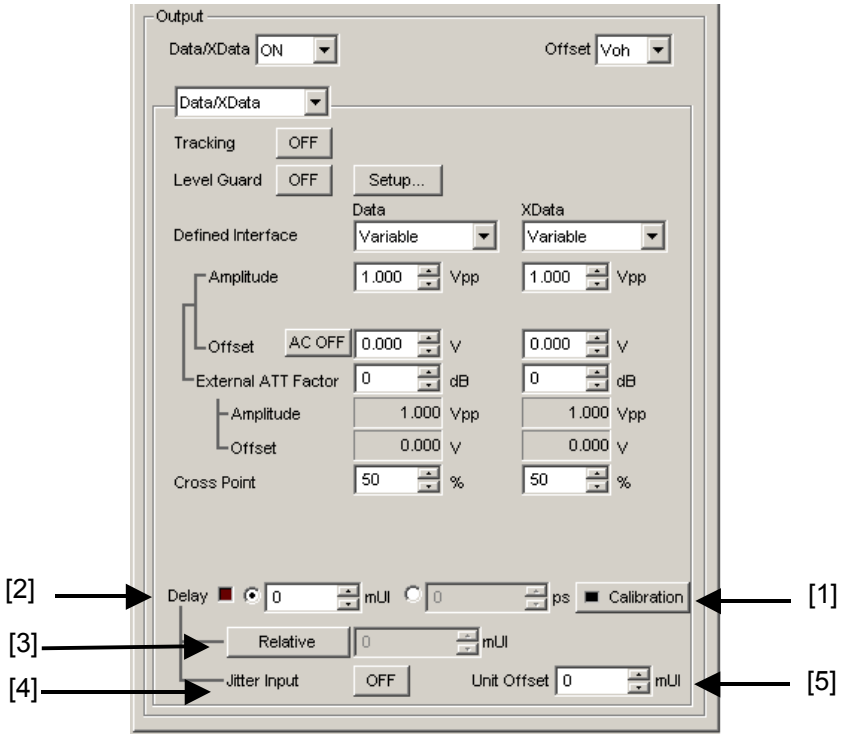


Figure 5.1.2-2 Delay Setting Screen for Output Tag

[1] Click [Calibration] to perform calibration, which is a phase variable function. When the power is supplied, the frequency is changed, or the ambient temperature fluctuates, the calibration prompting alarm LED lights up. In such a case, click this button to perform calibration. Calibration will finish within 1 second.

[2] Set the delay in mUI or ps units.

<In the case of mUI units>
The delay can be set from –1000 to 1000 mUI, in 1-mUI steps.

With this equipment, the Data output phase can be varied relative to the Clock output when either the MU181020A-x30 or MU181020B-x30 is installed. When the 2 Ch Combination, 4 Ch Combination, or Channel Synchronization option is installed, setting is supported from –64,000 to 64,000 mUI in 1-mUI steps.

<In the case of ps units>
The delay can be set in steps of ps units, equivalent to 1 mUI. The setting range is the range converting –1000 to 1000 mUI in ps units.

During 2 Ch Combination, 4 Ch Combination or Channel Synchronization, the setting range is equivalent to the range when the unit is mUI (–64,000 to 64,000 mUI), converted into ps units.

Example:

Table 5.1.2-1 Delay setting range

Frequency	Setting range	
	Normal	2Ch Combination 4Ch Combination Channel Synchronization
12.5 GHz	–80 to 80 ps	–5120 to 5120 ps
4.25 GHz	–235 to 235 ps	–15,040 to 15,040 ps
100 MHz	–10,000 to 10,000 ps	–640,000 to 640,000 ps

[3] Click [Relative] to use the current set phase value as the reference of relative 0 for delay setting.

[4] Set the Jitter Input.
When inputting jitter-modulated clocks, set Jitter Input of Delay to ON. Refer to 5.1.5 “When setting jitter-modulated signals”.

[5] Set the Delay offset for each main frame.
This is enabled only when the Unit Sync setting is ON. The setting is the same for all MU181020A/B modules installed in the same main frame.
Set a value between –1000 and +1000 mUI in 1-mUI steps.
A value between –64,000 and +64,000 can be set in 1-mUI steps for Combination and Channel Synchronization.
However, due to the restrictions of the Delay setting in item [2], the setting range is Delay setting + Unit Offset setting = ±1000mUI (or ±64,000 mUI).

Refer to Appendix E of this manual for a description of how to use this function.

Notes:

- When the frequency or the temperature condition is changed, the LED on the [Calibration] lights, prompting performance of calibration. If calibration is not performed at this time, the error in the phase setting may be greater than at a normal phase setting.

- Values displayed in ps units vary as the frequency changes, because the MU181020A sets phases in mUI units as an internal standard.

5.1.2.1 Delay setting in the case of Combination or CH Synchronization

In the case of Combination or Channel Synchronization when multiple MU181020A modules are mounted, the delay between two or more slots can be changed relatively, as shown in Figure 5.1.2.1-1.

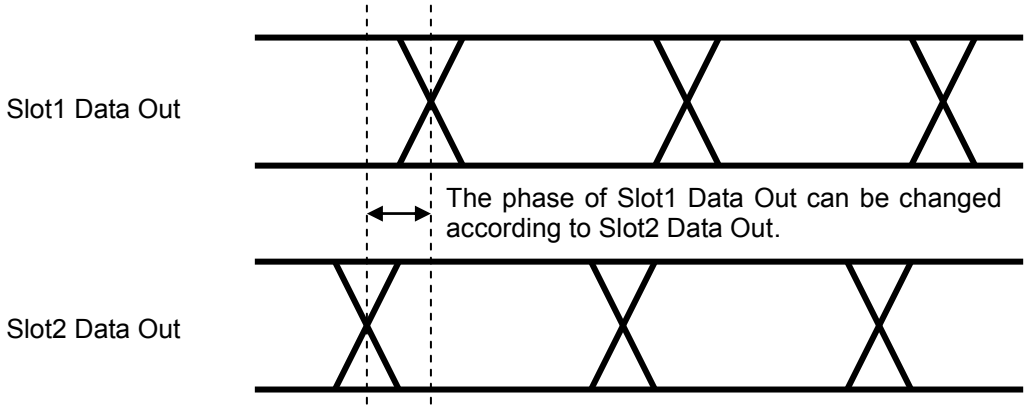


Figure 5.1.2.1-1 Delay setting in the case of Combination

5.1.3 Setting clock

Differential clock can be output when MU181020A-x30 or MU181020B-x30 is installed.

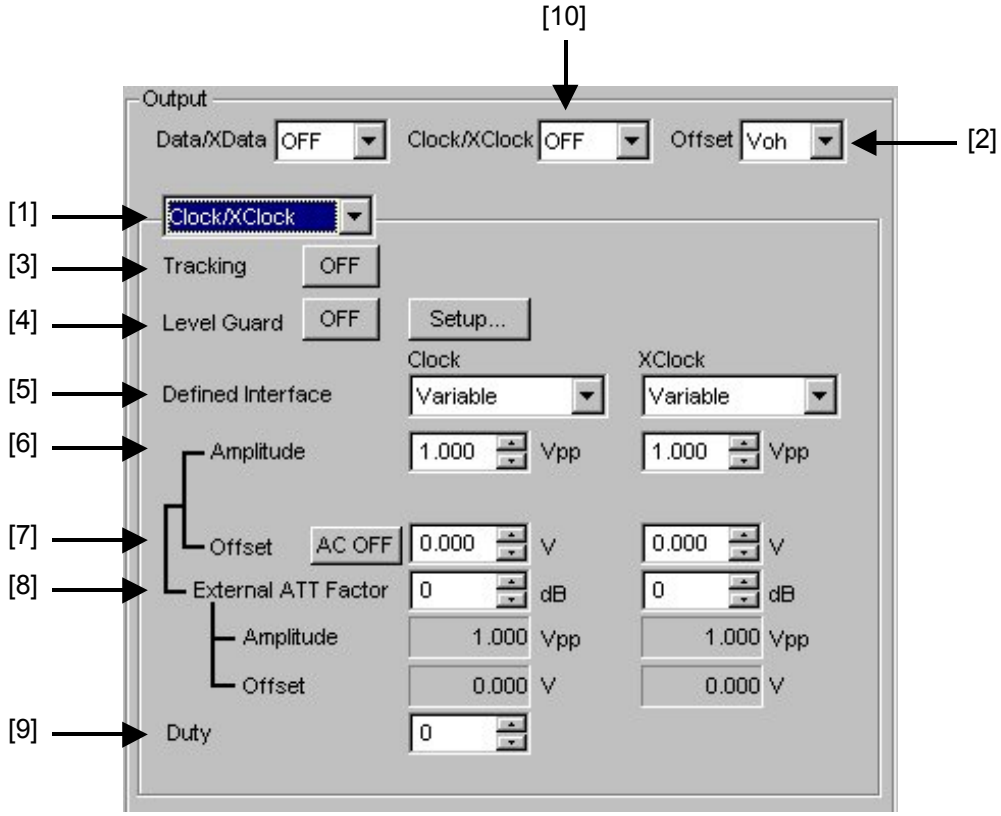


Figure 5.1.3-1 Output tab window for setting clock

[1] Select "Clock" or "XClock" from the list box.

[2] Select the offset reference from the list box. The setting range for the offset and amplitude is restricted by each setting value. Refer to Appendix A "Pseudo-Random Pattern (PRBS Pattern)" and Appendix C "Restrictions on Settings" for details on the setting ranges for the offset and amplitude. When the offset reference is changed, the offset value is calculated and changed based on the changed offset reference.

Table 5.1.3-1 Offset reference

Offset reference	Description
Voh	The offset value is set based on the high level.
Vth	The offset value is set based on the center level between the high and low levels.
Vol	The offset value is set based on the low level.

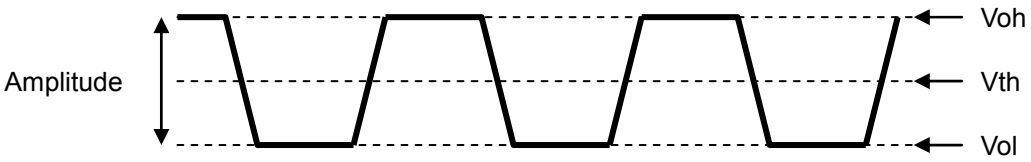


Figure 5.1.3-2 Setting clock offset

[3] Set Tracking ON/OFF. When Tracking is set to ON, the settings for the XClock become the same as those for the Clock.

[4] Configure the level guard setting. Click [Setup] to open the setup dialog box, and set the maximum amplitude, maximum offset (maximum value of the offset high level), and minimum offset (minimum value of the offset low level) for level guard, so that an excessively high voltage is not applied to the DUT.
When the external ATT factor is set (refer to [8] below), the level guard settings (Amplitude, Offset Max (Voh), and Offset Min (Vol)) after passing through the fixed attenuator, which is connected between the MU181020A and the DUT, limit the output level of these setting value. Therefore, if you use the fixed attenuator without connecting, a signal exceeding the setting value is output.

[5] Separately configure the defined interface setting for Clock and XClock.
Note that it may not be possible to select some items, depending on the level guard setting.

Table 5.1.3-2 Amplitude setting values

Item	Amplitude		Offset Vth
	Voh	Vol	
Variable	–	–	–
PCML	+3.3 V	+2.8 V	+3.05 V
NCML	0.0 V	–0.5 V	–0.25 V
SCFL	0.0 V	–0.9 V	–0.45 V
NECL	–0.9 V	–1.7 V	–1.3 V
LVPECL	+2.4 V	+1.6 V	+2.0 V
LVDS (200 mV)	+1.3 V	+1.1 V	+1.2 V
LVDS (400 mV)	+1.4 V	+1.0 V	+1.2 V

[6] Separately set the amplitude for Clock and XClock.
The setting range varies depending on the level guard setting and offset setting. The amplitude setting ranges when Defined Interface is set to Variable are shown in the table below.

Table 5.1.3-3 Amplitude setting range

Option	Amplitude	Setting steps
None	Fixed to 0.5 Vp-p	–
With x21 installed	0.1 to 2.0 Vp-p	0.002 V

[7] Separately set the offset for Clock and XClock.
The setting range varies depending on the level guard setting and amplitude setting. Click [AC OFF] to change it into [AC ON] to enable AC output.

Table 5.1.3-4 Offset setting range

Option	Offset	Setting steps	AC output
None	Fixed to 0.000 V (Offset: Vof)	–	Invalid
With x21 installed	–4.0 to 3.3 V	0.001 V	Valid

[8] Separately set the external ATT factor for Clock and XClock. When a fixed attenuator is connected to the Clock/XClock output connector of the MU181020A, the attenuation of the attenuator is added to the value for the DUT and displayed. A value from 0 to 40 dB can be set in 1-dB steps. When Defined Interface is not set to Variable, the setting is reset to 0 and becomes invalid. Values displayed in the External ATT Factor-Amplitude and Offset display areas indicates the amplitude and offset value after passing through the attenuator, respectively.

[9] Configure the duty setting. The duty can be set from –25 to 25, in single step.

[10] Set Output ON/OFF.
This setting applies for the selected MU181020A. When enabling the output signal (ON), enabling the output of all the instruments by clicking the Output module function button on the menu bar is also required.

Notes:

- The DUT may be damaged if the output setting is configured incorrectly. To prevent damage to the DUT, confirming the interface condition with the DUT, or configuring the level guard setting before making the output setting is recommended.

- When PCML, LVPECL, or NECL is selected for Defined Interface, the voltage corresponding to the DUT's termination voltage is applied to the output side of the MU181020A. In this event, the DUT may be damaged if the interface conditions do not match. Be sure to confirm the interface conditions.

- Waveforms may be distorted (what is known as a ringing phenomenon) when a commercially-available ECL terminator is used to observe output waveforms. This is, however, caused by the characteristics of the ECL terminator; the waveform output from the mainframe is not distorted.

- The current for the output part is limited (50 mA for sourcing current and 80 mA for sinking current) for protection. If an overcurrent flows due to the wrong interface condition, the offset voltage for an observed waveform may therefore not reach the set level.

- Be sure to confirm that a fixed attenuator is connected between the MU181020A and the DUT before setting the external ATT factor. If the external ATT factor is set when no fixed attenuator is connected or when the fixed attenuator has an attenuation value less than that set in the External ATT Factor area, the DUT may be damaged.

5.1.4 Setting CMU Bit-rate

When the MU181020A-001 is installed into the MU181020A, the CMU bit-rate can be set. An external synthesizer is therefore not required in this event.

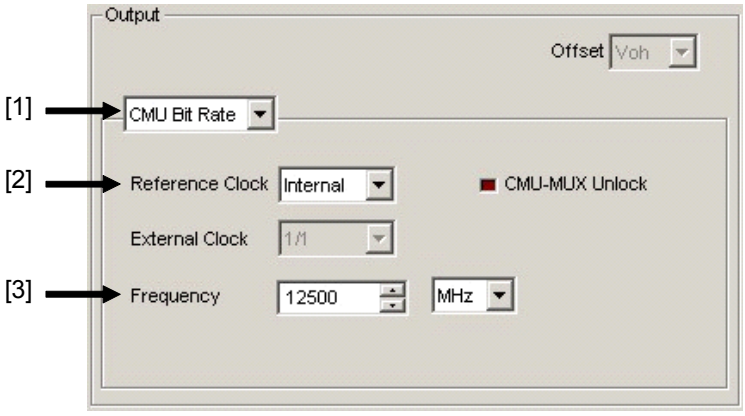


Figure 5.1.4-1 Output tab window for setting CMU Bit-rate (Internal)

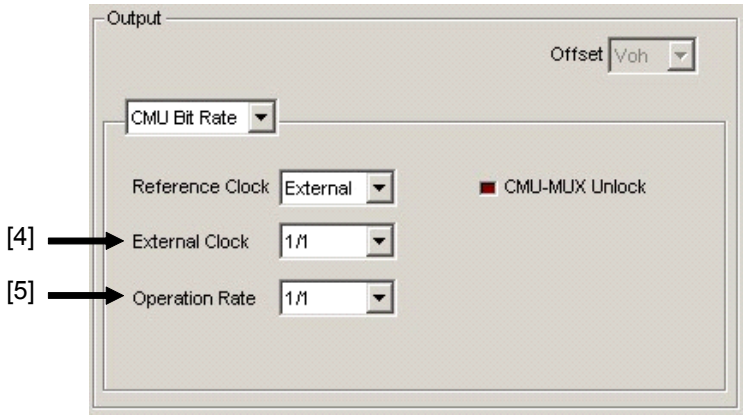


Figure 5.1.4-2 Output tab window for setting CMU Bit-rate (External)

[1] CMU Bit-rate can be selected from the list box.

[2] Select the internal clock or external clock for the CMU reference clock from the Reference Clock list box.

Table 5.1.4-1 Reference clock setting

Reference Clock	Description
Internal	The internal clock is used as the CMU reference clock. Set the frequency in the Frequency text box and the unit from the list box ([3] in Figure 5.1.4-1).
External	The external input clock is used as the CMU reference clock. Input the reference clock via the Ext. Clock Input connector of the MU181020A.

[3] When "Internal" is selected for Reference Clock, set the frequency to be generated.

Set the frequency of the output signal when "Internal" is selected for Reference Clock ([1] in Figure 5.1.4-1).
The setting range is as follows.

Table 5.1.4-2 Output frequency setting

Unit	Setting range	Resolution
MHz	1225 to 1562	1 MHz
	2450 to 3125	
	4900 to 6250	
	9800 to 12500	
kHz	1225000 to 1562500	1 kHz
	2450000 to 3125000	
	4900000 to 6250000	
	9800000 to 12500000	

[4] When "External" is selected for Reference Clock, set the rate of the reference clock.

Table 5.1.4-3 External clock rate setting

External Clock	Description
1/1	The data signal and clock signal with the same rate as that of the external input clock are generated. The range of the frequency for the external input clock is from 9,800 to 12,500 MHz.
1/64	The data signal and clock signal with the external input clock's rate multiplied by 64 are generated. The range of the frequency for the external input clock is from 9,800/64 to 12,500/64 MHz (i.e., 153.125 to 195.3125 MHz).

[5] When "External" is selected for Reference Clock, the rate of the output data signal can be set from the Operation Rate list box.

Set the rate of the output data signal when "External" is selected for Reference Clock ([1] in Figure 5.1.4-1).

(a) When External Clock is set to 1/1

Table 5.1.4-4 Operation rate setting (when external clock is 1/1)

Operation Rate	Data signal output rate
1/1	Output rate for external input clock (9.8 to 12.5 GHz)
1/2	1/2 of output rate for external input clock (4.9 to 6.25 GHz)
1/4	1/4 of output rate for external input clock (2.45 to 3.125 GHz)
1/8	1/8 of output rate for external input clock (1.225 to 1.5625 GHz)

(b) When External Clock is set to 1/64

Table 5.1.4-5 Operation rate setting (when external clock is 1/64)

Operation Rate	Data signal output rate
1/1	64 times of output rate for external input clock (9.8 to 12.5 GHz)
1/2	32 times of output rate for external input clock (4.9 to 6.25 GHz)
1/4	16 times of output rate for external input clock (2.45 to 3.125 GHz)
1/8	8 times of output rate for external input clock (1.225 to 1.5625 GHz)

5.1.5 When setting jitter-modulated signals

- When inputting jitter-modulated clocks, set Jitter Input of Delay to ON. (Refer to Figure 5.1.5-1.) When using the MU181000A/B (with Option 001 Jitter Modulation), set Jitter Input of Delay to ON, and then set Jitter Modulation of the MU181000A/B to ON.
- Set the jitter modulation for input signals to non-modulation when executing calibration of Delay.
- When configuring Combination Setting, set the jitter modulation to non- modulation before setting Combination or Channel Synchronization.
- When changing the input frequency while Combination or Channel Synchronization is set, be sure to set Jitter Input of Delay for the MU181020A to ON and then set the jitter modulation to ON, in this order, after changing the frequency for measurement.

Figure 5.1.5-1 Output tab window for setting delay

Notes:

- When jitter-modulated clock is input while Jitter Input of Delay is set to OFF, the phase may become unstable.
- The Delay lamp may light up when a jitter-modulated clock signal is input. In addition, phase setting error may increase.

5.2 Setting Test Patterns

Click the [Pattern] tab on the operation tab window to open the Pattern tab window. A test pattern can be selected and set in this window.

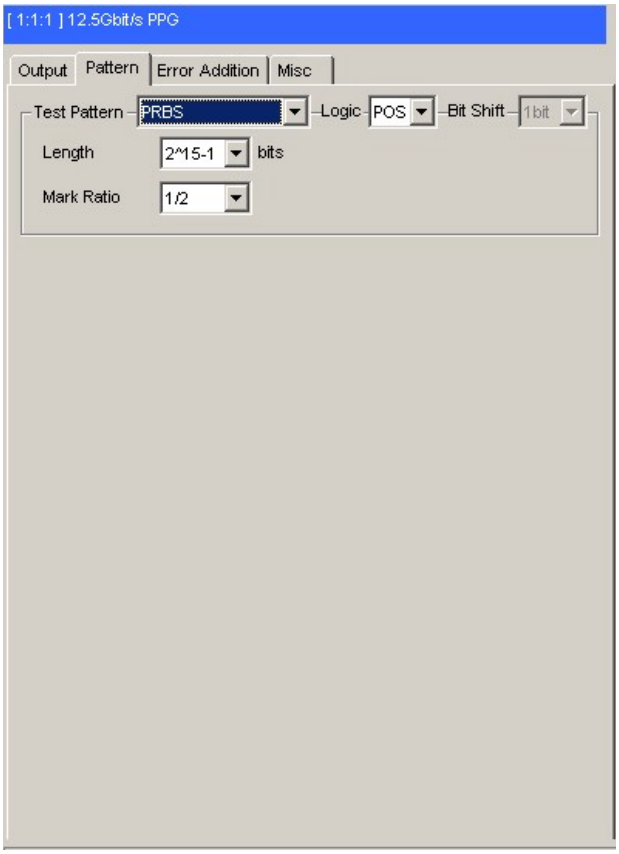


Figure 5.2-1 Pattern tab window

5.2.1 Test pattern type

The following six test patterns can be selected.

- PRBS
- Zero-Substitution
- Data
- Alternate
- Mixed
- Sequence

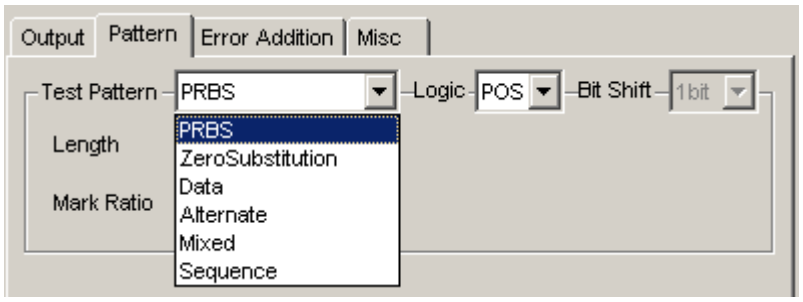


Figure 5.2.1-1 Selecting test pattern

How to set each test pattern is described in the subsequent sections.

5.2.2 Setting PRBS pattern

This section describes how to set the parameters required when PRBS is selected as the test pattern.

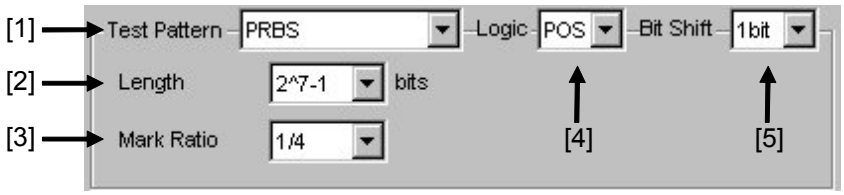


Figure 5.2.2-1 Setting items for PRBS pattern

[1] Select "PRBS" from the Test Pattern list box.

[2] Set the number of the PRBS pattern stages.

Set the PRBS pattern length in the format of $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31).

[3] Select the mark ratio.

The selectable mark ratios vary depending on the logic setting (PRBS Logic).
When Logic is set to POS, 1/2, 1/4, 1/8, and 0/8 can be selected.
When Logic is set to NEG, 1/2inv, 3/4, 7/8, and 8/8 can be selected.

[4] Set the logic of the test pattern.

Table 5.2.2-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "0".
NEG (negative logic)	The high level of a signal is defined as "1".

[5] Set the bit shift.
In order to change the correlation between the bit patterns at the change of the PRBS signal mark ratio, the pattern is shifted by the value set here when passing through the AND gate.
"1 bit" or "3 bit" can be selected.
This setting is valid only when the mark ratio setting is valid and set to 1/4 (3/4) or 1/8 (7/8).

Refer to Appendix A "Pseudo-Random Pattern (PRBS Pattern)" for the PRBS pattern generation principle.

5.2.3 Setting Zero-substitution pattern

This section describes how to set the parameters required when Zero-Substitution is selected as the test pattern.

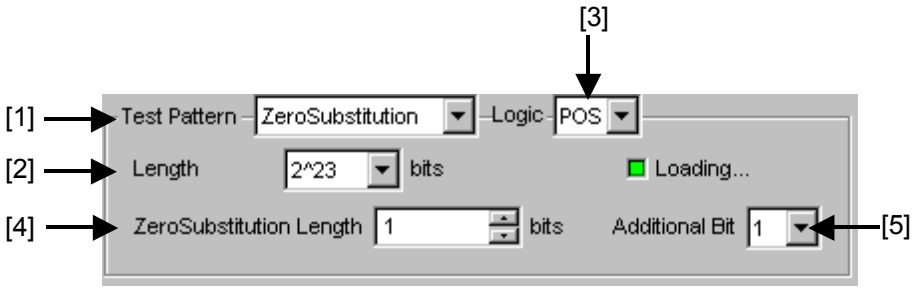


Figure 5.2.3-1 Setting items for Zero-substitution pattern

[1] Select "Zero Substitution" from the Test Pattern list box. Test pattern loading starts and the "Loading…" LED lights.

[2] Set the configuration (number of stages) of the zero-insertion pattern test signal.

Select either of the following test pattern signals.
2^n (n = 7, 9, 10, 11, 15, 20, or 23) [Compatible with the existing models]
$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, or 23) [Pure PRBS signal]

[3] Set the logic of the test pattern.

Table 5.2.3-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[4] Set the number of 0-insertion (substitution) bits in the zero-insertion (substitution) pattern.

The number of available 0-insertion bits varies depending on the pattern test signal selected from the Length list box ([2] in Figure 5.2.3-1) as follows.

(a) When $2^n - 1$ is set for Length: 1 to $2^n - 2$, in 1-bit steps

(b) When 2^n is set for Length: 1 to $2^n - 1$, in 1-bit steps

[5] Set the final bit of the zero-insertion pattern. Note that this setting is invalid when Length is set to $2^n - 1$.

Table 5.2.3-2 Setting of last bit of zero-insertion pattern

Setting	Description
1	The 2^nth bit is set to "1" (compatible with the existing models).
0	In order to make an M-series signal, 1 bit of "0" is added to the last of consecutive 0 strings to configure a zero-insertion pattern.

5.2.4 Setting Data pattern

This section describes how to set the parameters required when Data is selected as the test pattern.

Figure 5.2.4-1 Setting items for Data pattern

[1] Select "Data" from the Test Pattern list box. Test pattern loading starts and the "Loading…" LED lights.

[2] Set the logic of the test pattern.

Table 5.2.4-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[3] Click [Edit] to open the Pattern Editor dialog box in which test patterns can be edited.
When editing of a test pattern is finished, click [OK] to close the Pattern Editor dialog box. The edited test pattern is then loaded to the hardware. The "Loading…" LED lights during Data pattern loading. Refer to Section 5.2.8 "Editing test pattern in Pattern Editor dialog box" for details on how to edit test patterns in the Pattern Editor dialog box.

[4] The length of the test pattern data currently set is displayed.

Note:

It may take a long time to load a test pattern when the data length is long.

5.2.5 Setting Alternate pattern

When "Alternate" is selected and two test patterns A and B are set, these test patterns can be alternately output for the specified number of times. Selection is disabled when Combination or Burst is set.

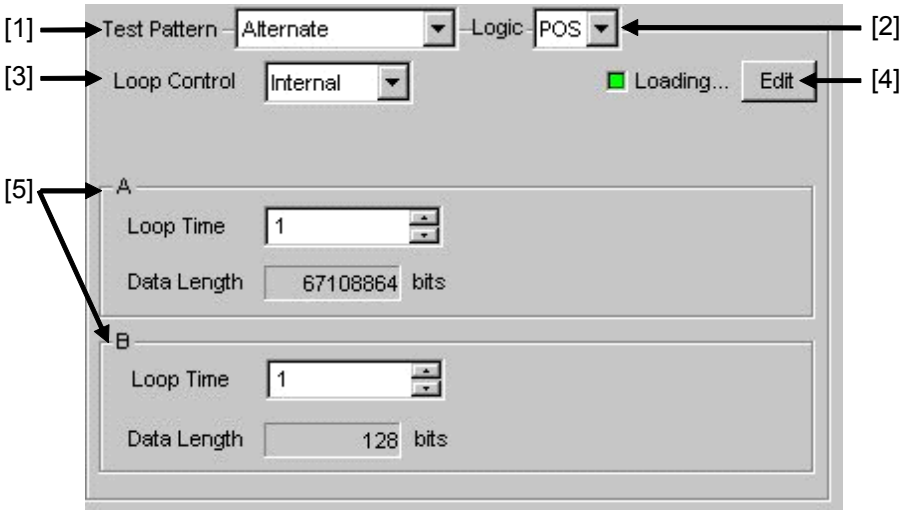


Figure 5.2.5-1 Setting items for Alternate pattern

[1] Select "Alternate" from the Test Pattern list box. Test pattern loading starts and the "Loading…" LED lights.

[2] Set the logic of the test pattern.

Table 5.2.5-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as "1".
NEG (negative logic)	The high level of a signal is defined as "0".

[3] Select from the Loop Control list box the control method for switching between the alternate test patterns A and B.

Table 5.2.5-2 Switching control method setting

Setting	Description
Internal	The alternate test patterns A and B are alternately output according to the settings in [5] in Figure 5.2.5-1.
External	Switching between the alternate test patterns A and B is controlled by the external Alternate Control signal. "Alternate Control" must be selected from the AUX Input list box on the Misc tab window.
Manual	The [Manual] is displayed when Manual is selected. When [Manual] is clicked, the test pattern output is switched from A to B. When the test pattern B is output for the number of times specified in the Loop Time textbox in the B area, test pattern A output is resumed.

[4] Edit the alternate test patterns A and B.
Click [Edit] to open the Pattern Editor dialog box, in which alternate test patterns A and B can be edited. When editing of a test pattern is finished, click [OK] to close the Pattern Editor dialog box. The edited test pattern is then loaded to the hardware. The "Loading…" LED lights during Data pattern loading. Refer to Section 5.2.8 "Editing test pattern in Pattern Editor dialog box" for how to edit test patterns in the Pattern Editor dialog box.

[5] Separately set the loop time for test patterns A and B.
Specify the repetition number of pattern output times for test pattern A or B. The loop time can be set from 1 to 511 (times), in 1-time steps. Note that this parameter cannot be set when Alternate Loop Control is set to External. Also, the loop time cannot be set for the alternate test pattern A when Alternate Loop Control is set to Manual.

The length of the test pattern edited in the Pattern Editor dialog box is displayed in the Data Length textbox in the A and B areas.

Notes:

- "Alternate" cannot be selected from the Test Pattern list box when a Burst pattern is output.
  On the other hand, Burst cannot be selected from the Pattern Sequence list box on the Misc tab window when Alternate is selected from the Test Pattern list box.

- It may take a long time to load a test pattern when the data length is long.

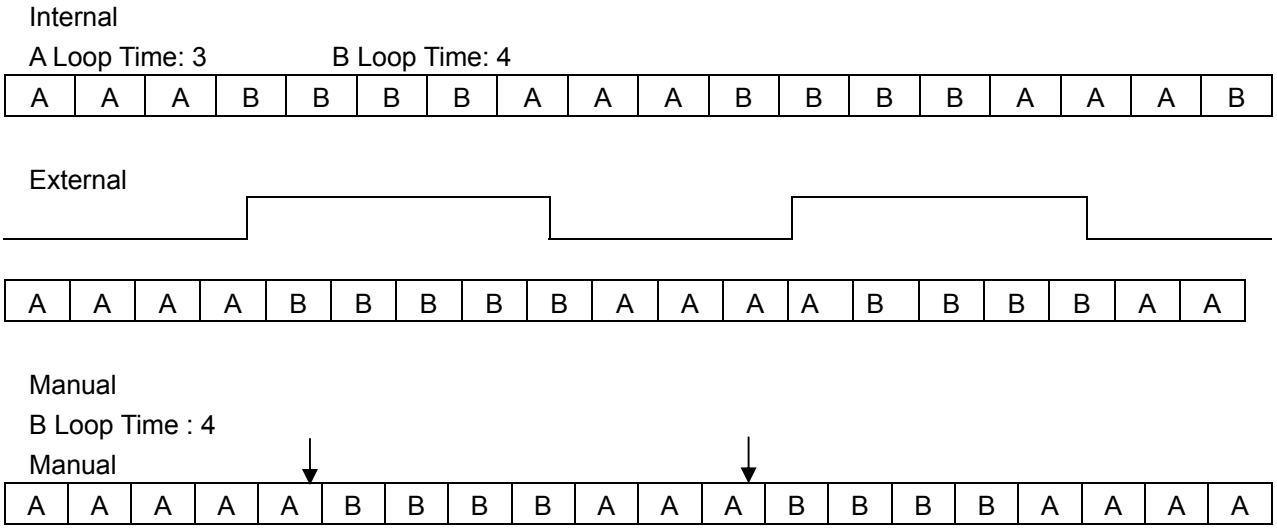


Figure 5.2.5-2 Alternate test pattern switching example

5.2.6 Setting Mixed pattern

When "Mixed" is selected, a block consisting of programmable test patterns and PRBS patterns can be set.

5.2.6.1 Setting Mixed Data pattern

A programmable test pattern added with a PRBS pattern is defined as "row", one block is composed of two or more rows. A mixed data test pattern is set by configuring multiple blocks.

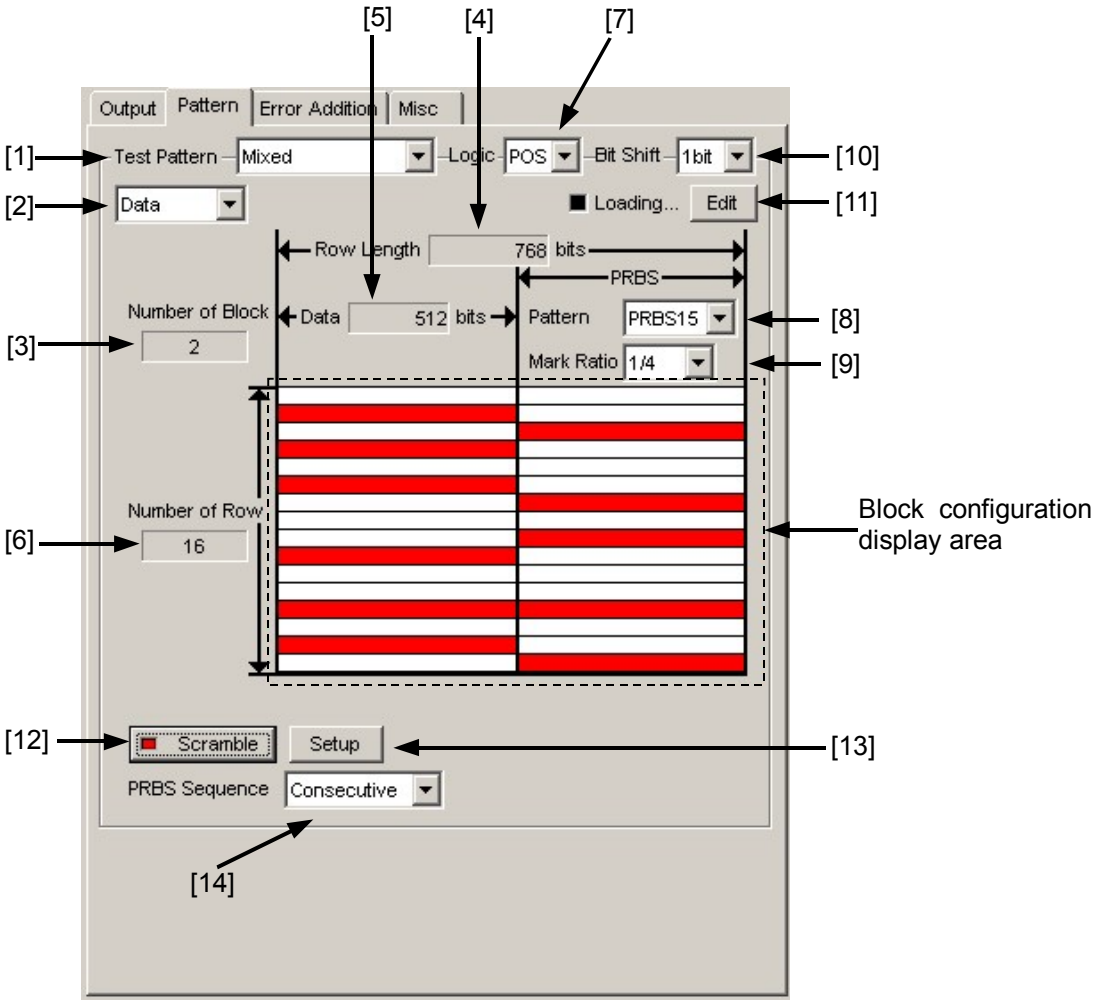


Figure 5.2.6.1-1 Setting items for Mixed Data pattern

[1] Select "Mixed" from the Test Pattern list box.

[2] Select "Data" from the list box.
When "Data" is selected, each row within a block is configured with a programmable test pattern and a PRBS pattern.

[3] Number of Block
The number of all blocks in the pattern data edited in the Pattern Editor dialog box is displayed. The maximum number of blocks is 511.

[4] Row Length
The length of 1 row of the pattern data edited in the Pattern Editor dialog box is displayed.

[5] Data Length
The length of the Data pattern edited in the Pattern Editor dialog box is displayed.

[6] Number of Row
The number of rows in one block of the pattern data edited in the Pattern Editor dialog box is displayed.

[7] Set the logic of the test pattern.

Table 5.2.6.1-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

[8] Set the number of the PRBS pattern stages.

Set the PRBS pattern length in the format of $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31).

[9] Select the mark ratio.

The selectable mark ratios vary depending on the logic setting (PRBS Logic).
When Logic is set to POS, 1/2, 1/4, 1/8, and 0/8 can be selected.
When Logic is set to NEG, 1/2inv, 3/4, 7/8, and 8/8 can be selected.

[10] Set the bit shift.
In order to change the correlation between the bit patterns at the change of the PRBS signal mark ratio, the pattern is shifted by the value set here when passing through the AND gate.
“1bit” or “3bit” can be selected.
This setting is valid only when the mark ratio setting is valid and set to 1/4 (3/4) or 1/8 (7/8).

[11] Click [Edit] to open the Pattern Editor dialog box in which test patterns can be edited.
When editing of a test pattern is finished, click [OK] to close the Pattern Editor dialog box. The edited test pattern is then loaded to the hardware. The "Loading…" LED lights during test pattern loading. Refer to Section 5.2.8 "Editing test pattern in Pattern Editor dialog box" for details on how to edit test patterns in the Pattern Editor dialog box.

Note:

It may take a long time to load a test pattern when the data length is long.

[12] Set scramble ON/OFF.

PRBS7 scramble can be executed for the part of the test pattern. When [Scramble] is clicked while the LED on the button is off, the LED lights and scramble is executed for the output signal. The scramble area set from the [Setup] is displayed red in the block configuration display area.
When [Scramble] is clicked while the LED on the button is on, the LED goes off and scramble for the output signal is stopped.

[13] Configure the scramble settings.
Clicking [Setup] opens the Scramble Setup dialog box. Select the checkbox for the target area for scramble. After selecting the target area(s), click [OK].

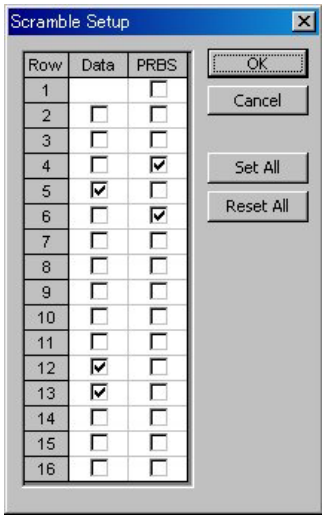


Figure 5.2.6.1-2 Scramble Setup dialog box

Note:

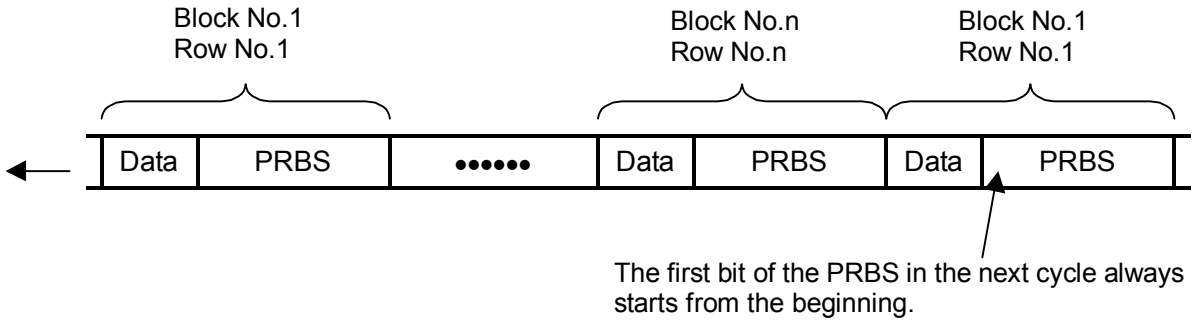
Scramble cannot be set for the data area of the first row in each block.

[14] Set the PRBS signal generation method.
Set the continuity of the PRBS pattern strings in a Mixed pattern.

Table 5.2.6.1-2 PRBS signal generation method setting

Setting	Description
Restart	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are not continuous.
Consecutive	The end of the PRBS of the specified last block and the start of the PRBS of the next subsequent block are not continuous.

(a) When Restart is selected



(b) When Consecutive is selected

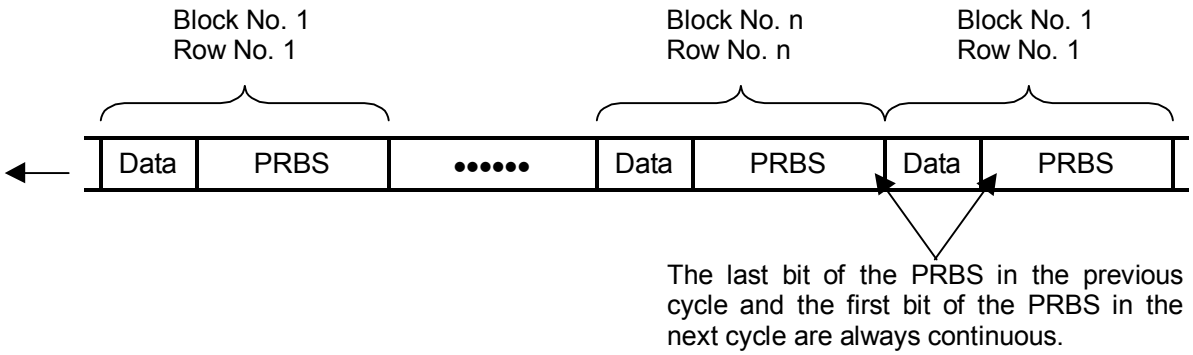


Figure 5.2.6.1-3 Continuity of PRBS pattern strings

5.2.6.2 Setting Mixed Alternate pattern

A programmable test pattern added with a PRBS pattern is defined as a "row", and one block is composed of two or more rows. A Mixed Data test pattern is configured by multiple blocks, and a Mixed Alternate test pattern is set by configuring two types of Mixed Data test patterns, A and B. The test patterns A and B can be output alternately for the specified number of times. Selection is disabled when Combination or Burst is set.

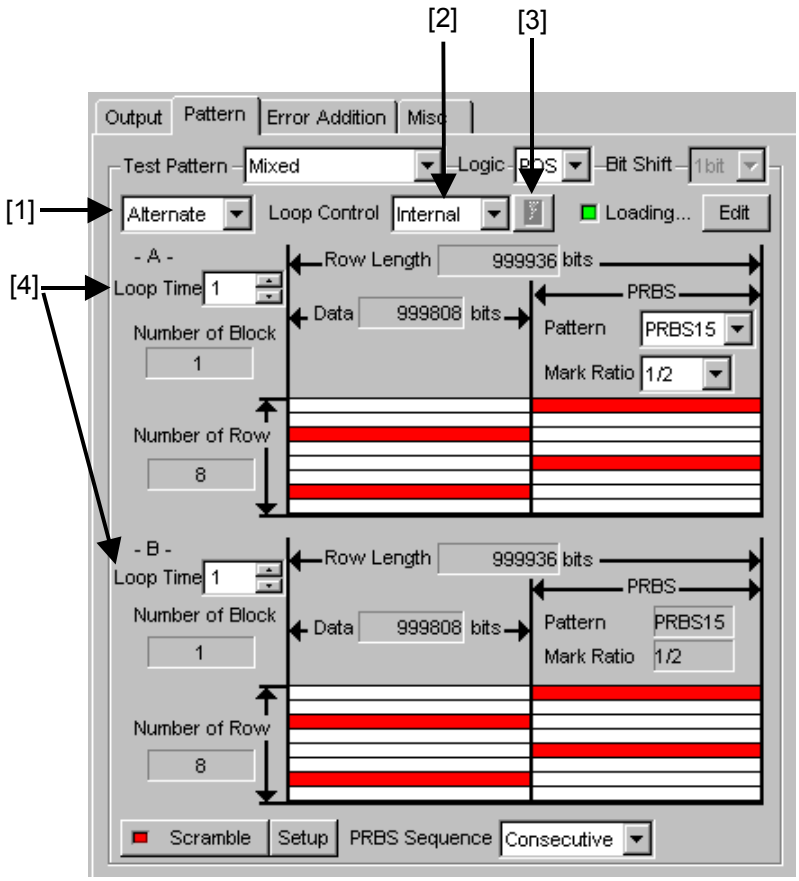


Figure 5.2.6.2-1 Setting items for Mixed Alternate pattern

[1] Select "Alternate" from the list box.
When "Alternate" is selected, set two types of Mixed Data test patterns, A and B.

[2] Select from the Loop Control list box the control method for switching between the alternate test patterns A and B.

Table 5.2.6.2-1 Switching control method setting

Setting	Description
Internal	The alternate test patterns A and B are alternately output according to the settings in [4] in Figure 5.2.6.2-1.
External	Switching between the alternate test patterns A and B is controlled by the external Alternate Control signal. "Alternate Control" must be selected from the AUX Input list box on the Misc tab window.
Manual	The [Manual] is displayed when Manual is selected. When [Manual] is clicked, the test pattern output is switched from A to B. When the test pattern B is output for the number of times specified in the Loop Time textbox in the B area, test pattern A output is resumed.

[3] The [Manual] becomes enabled when is set Manual is selected from the Loop Control list box. When [Manual] is clicked, the test pattern output is switched from A to B. When the test pattern B is output for the number of times specified in the Loop Time textbox in the B area, test pattern A output is resumed.

[4] Separately set the loop time for test patterns A and B.
Specify the repetition number of pattern output times for test pattern A or B. The loop time can be set from 1 to 511 (times), in 1-time steps. Note that this parameter cannot be set when Alternate Loop Control is set to External. Also, the loop time cannot be set for the alternate test pattern A when Alternate Loop Control is set to Manual.

The length of the test pattern edited in the Pattern Editor dialog box is displayed in the Data Length textbox in the A and B areas.

Note:

"Alternate" cannot be selected from the Test Pattern list box when a Burst pattern is output.
On the other hand, Burst cannot be selected from the Pattern Sequence list box on the Misc tab window when Alternate is selected from the Test Pattern list box.
It may take a long time to load a test pattern when the data length is long.

5.2.7 Setting Sequence pattern

When “Sequence” is selected from the Test Pattern list box, it is possible to set a signal pattern that transmits up to 128 patterns (blocks) in the pre-defined order. Selection is disabled when Combination or Burst is set.

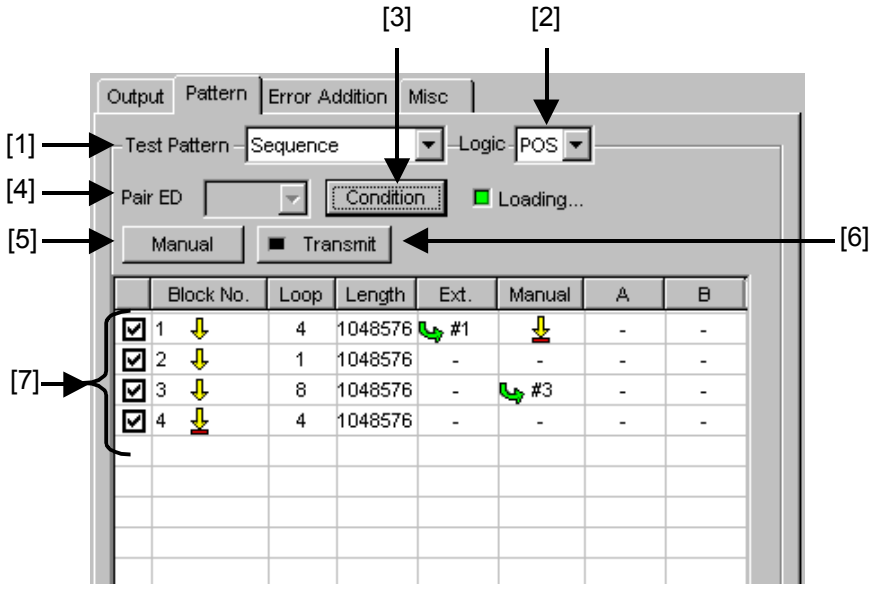


Figure 5.2.7-1 Setting items for Sequence pattern

[1] Select “Sequence” from the Test Pattern list box.

[2] Set the logic of the test pattern.

Table 5.2.7-1 Test pattern logic setting

Setting	Description
POS (positive logic)	The high level of a signal is defined as “1”.
NEG (negative logic)	The high level of a signal is defined as “0”.

[3] Click [Condition] to open the Sequence Pattern Setting dialog box. In this dialog box, a pattern transmission sequence scenario that registers patterns, configures pattern settings, and defines the transmission order and the number of transmission repetition times, can be set.

[4] When the transmitted signals are received via DUT by MU181040A or MU181040B (hereinafter, MU181040A/B), which is mounted in the same unit, set Pair ED when there is a pair of MU181040A/B. When the specified pattern is detected by the pair MU181040A/B, the sequence moves to the next transit condition.

Note:

When the test pattern is changed to other than Sequence, the Pair ED setting is reset to “None”.
Set the same test pattern data for each block and the same number of registered blocks for both the MU181020A and the MU181040A/B. Otherwise, measurement may not be performed correctly.

[5] When Manual Trigger is set as a sequence transit condition of the sequence scenario set in the Sequence Pattern Setting dialog box, clicking [Manual] transmits the next test pattern.

[6] Click [Transmit] to output a sequence pattern again from Block 1. The LED on the [Transmit] lights up for about 2 seconds after the button is clicked. The [Transmit] should also be clicked to output a sequence pattern after setting data is loaded from a setting file.

[7] The set sequence pattern is displayed in this area.

5.2.7.1 Setting conditions for Sequence pattern

Clicking [Condition] on the Pattern tab window for setting a sequence test pattern opens the Sequence Pattern Setting dialog box. Click [OK] to apply the settings and close this dialog box. Click [Cancel] to cancel the settings and close this dialog box. The set sequence pattern is output when this dialog box is closed.

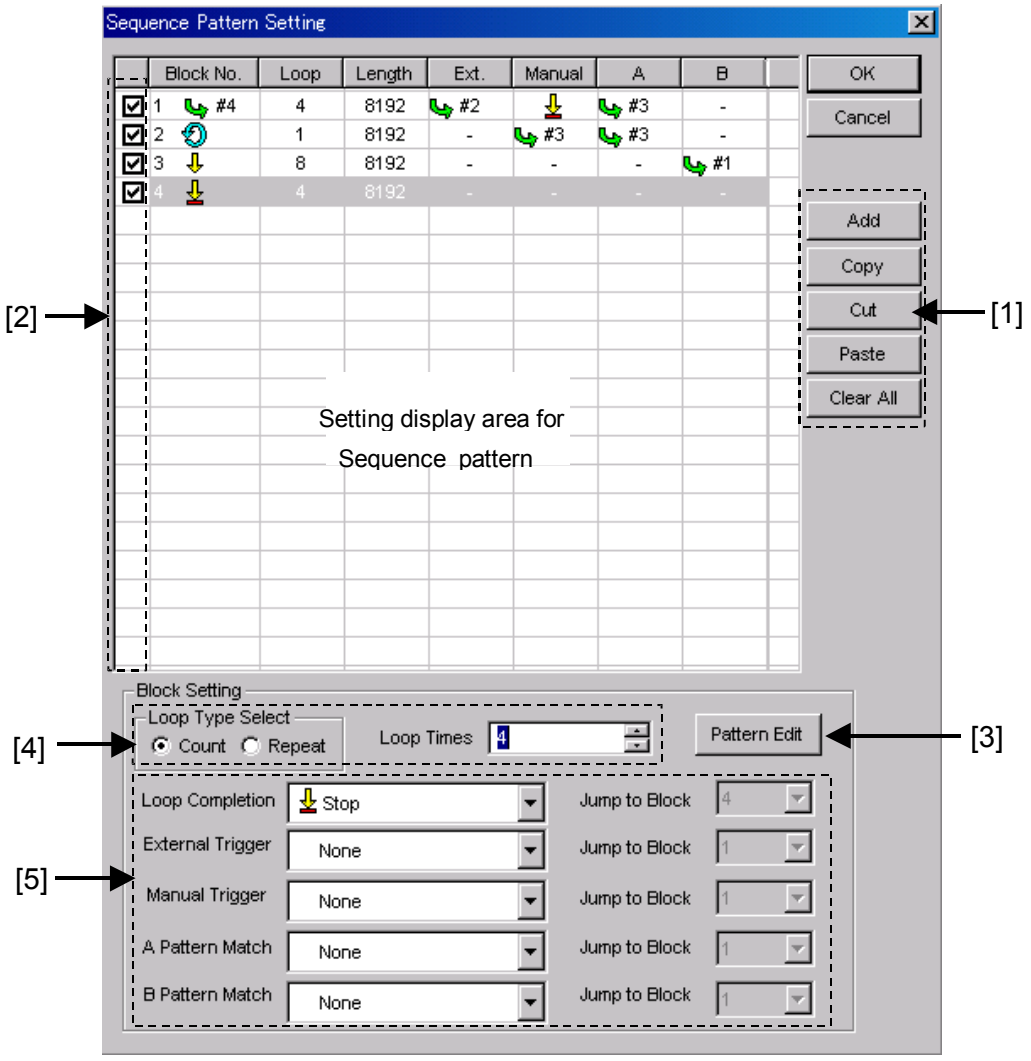


Figure 5.2.7.1-1 Sequence Pattern Setting dialog box

[1] Buttons used to set the transmission sequence.

Table 5.2.7.1-1 Transmission sequence setting button

Button	Description
Add	Click to add a block to the Sequence pattern being set.
Copy	Click to copy the block selected in the sequence pattern setting display area.
Cut	Click to copy and cut out the block selected in the sequence pattern setting display area.
Paste	Click to paste the block that is copied or cut in the sequence pattern setting display area between the selected block and the previous block.
Clear All	Click to delete all the blocks of the sequence pattern displayed in the sequence pattern setting display area.

[2] Transmission of a block can be canceled by clearing the corresponding checkbox.

Note:

Note that an undefined value may be output when all blocks are cleared using the [Cut] or [Clear All], or when transmission of a block is canceled by clearing the corresponding checkbox.

[3] In the Sequence Pattern Setting dialog box, select a block to set the test pattern and click [Pattern Edit] to open the Pattern Editor dialog box. The test patterns of the selected block can be edited in this dialog box. Refer to Section 5.2.8 “Editing test pattern in Pattern Editor dialog box” for how to edit test patterns in the Pattern Editor dialog box.

[4] Set the loop type.

Table 5.2.7.1-2 Loop type setting

Setting	Description
Count	The data of the block selected in the sequence pattern setting display area is repeatedly transmitted for the number of times set in the Loop Times list box.
Repeat	The data of the block selected in the sequence pattern setting display area is repeatedly transmitted until an External Trigger or Manual Trigger condition is satisfied.

[5] Set the transit conditions for the transmission sequence of each block.

Table 5.2.7.1-3 Transition condition setting

Transit condition	Description
Loop Completion	This is enabled when Count is selected for Loop Type Select. Set the transition method after the data of the block selected in the sequence pattern setting display area is transmitted for the number of times set in the Loop Times list box, from Stop, Jump, and Next. When setting Jump, select the block to be transmitted next from the Jump to Block list box.
External Trigger	For the block selected in the sequence pattern setting display area, set the transit condition when an external trigger is detected, from Stop, Jump, Next, and None. When setting Jump, select the block to be transmitted next from the Jump to Block list box. An external trigger signal is output from the AUX Input connector. When setting the external trigger, select "Sequence Control" from the AUX Input list box in the Misc. tab window. When inputting external trigger signals in succession, the input period must be 8192 bits or longer and the pulse width must be 64/Data output frequency or longer.
Manual Trigger	For the block selected in the sequence pattern setting display area, set the transition method when [Manual] is clicked, from Stop, Jump, Next, and None. When setting Jump, select the block to be transmitted next from the Jump to Block list box.
A Pattern Match	Set the transition method when a pattern matches the match pattern, which is set as the match pattern A condition in the Pattern tab window with Test Pattern "Sequence" of the MU181040A/B (selected from the Pair ED list box in the Pattern tab window).
B Pattern Match	Set the transition method when a pattern matches the match pattern, which is set as the match pattern B condition in the Pattern tab window with Test Pattern "Sequence" of the MU181040A/B (selected from the Pair ED list box in the Pattern tab window).

Note:

When setting A Pattern Match or B Pattern Match for the transit condition with Count selected for Loop Type Select, set the loop time to be 5 or greater from the Loop Times list box. If the loop time is set to 4 or less, transition may not be performed normally.

Select one of the following transit methods for each transit condition.

Table 5.2.7.1-4 Transition method setting

Transit method	Description
Stop	The pattern transmission is stopped when the transit condition is detected. In this state, 0 is output from the Data connector and 1 is output from the XData connector respectively.
Jump	The pattern of the block set in the Jump to Block list box is transmitted when the transit condition is detected.
Next	The pattern of the next block number is transmitted when the transit condition is detected.
None	No operation is performed, even when the transit condition is detected.

5.2.7.2 Specific example of setting Sequence pattern

A specific example of creating a scenario with a Sequence pattern is described below, using the settings in the Sequence Pattern Setting dialog box shown in Figure 5.2.7.1-1.

1. Click [Add] four times to add four blocks.
2. Select Block No. 1 and set as follows.

Table 5.2.7.2-1 Sequence pattern setting example (Block No. 1)

Item	Setting
Loop Type Select	Count
Loop Times	5
Loop Completion	Specify "Jump" and select "4" from Jump to Block list box.
External Trigger	Specify "Jump" and select "2" from Jump to Block list box.
Manual Trigger	Stop
A Pattern Match	Specify "Jump" and select "3" from Jump to Block list box.
A Pattern Match	None

In Figure 5.2.7.1-1, the sequence starts from Block No. 1 when [Transmit] is clicked. The loop time is set to "5", so when the pattern of Block No. 1 is transmitted five times, the sequence jumps to Block No. 4. At this time, if an external trigger is detected while the pattern of Block No. 1 is being transmitted, the sequence jumps to Block No. 2. If a manual trigger is detected in the middle of the Block No. 1 pattern transmission, the sequence stops. If a pattern matches the A Pattern set in the MU181040A/B (selected from the Pair ED list box), the sequence jumps to Block No. 3.

3. Select Block No. 2 and set as follows.

Table 5.2.7.2-2 Sequence pattern setting example (Block No. 2)

Item	Setting
Loop Type Select	Repeat
External Trigger	None
Manual Trigger	Specify "Jump" and select "3" from Jump to Block list box.
A Pattern Match	Specify "Jump" and select "3" from Jump to Block list box.
A Pattern Match	None

When the sequence has transited to Block No. 2 due to a transit condition, the Repeat radio button is selected for Loop Time Select at this time, so the pattern of Block No. 2 is transmitted repeatedly until another trigger condition is detected. If [Manual] is clicked while the pattern of Block No. 2 is being transmitted, the sequence jumps to Block No. 3. Similarly, if a pattern matches the A Pattern set in the MU181040A/B (selected from the Pair ED list box), the sequence jumps to Block No. 3.

4. Select Block No. 3 and set as follows.

Table 5.2.7.2-3 Sequence pattern setting example (Block No. 3)

Item	Setting
Loop Type Select	Count
Loop Times	8
Loop Completion	Next
External Trigger	None
Manual Trigger	None
A Pattern Match	None
A Pattern Match	Specify “Jump” and select “1” from Jump to Block list box.

The loop time is set to 8, so the sequence transits to Block No. 4 when the pattern of Block No. 3 is transmitted eight times. If a pattern that matches the B Pattern set in the MU181040A/B (selected from the Pair ED list box) is detected while the pattern of Block No. 3 is being transmitted, the sequence jumps to Block No. 1.

5. Select Block No. 4 and set as follows.

Table 5.2.7.2-4 Sequence pattern setting example (Block No. 4)

Item	Setting
Loop Type Select	Count
Loop Times	4
Loop Completion	Stop
External Trigger	None
Manual Trigger	None
A Pattern Match	None
A Pattern Match	None

The loop time is set to 4 in this example. The sequence stops when the pattern of Block No. 4 is transmitted four times.

5.2.8 Editing test pattern in Pattern Editor dialog box

Editing of test patterns with the following patterns selected in the Pattern tab window is described below.

[1] Data

[2] Alternate

[3] Mixed

[4] Sequence

5.2.8.1 Common setting items

The Pattern Editor dialog box is displayed when [Edit] or [Pattern Edit] (in the case of Sequence pattern) is clicked.

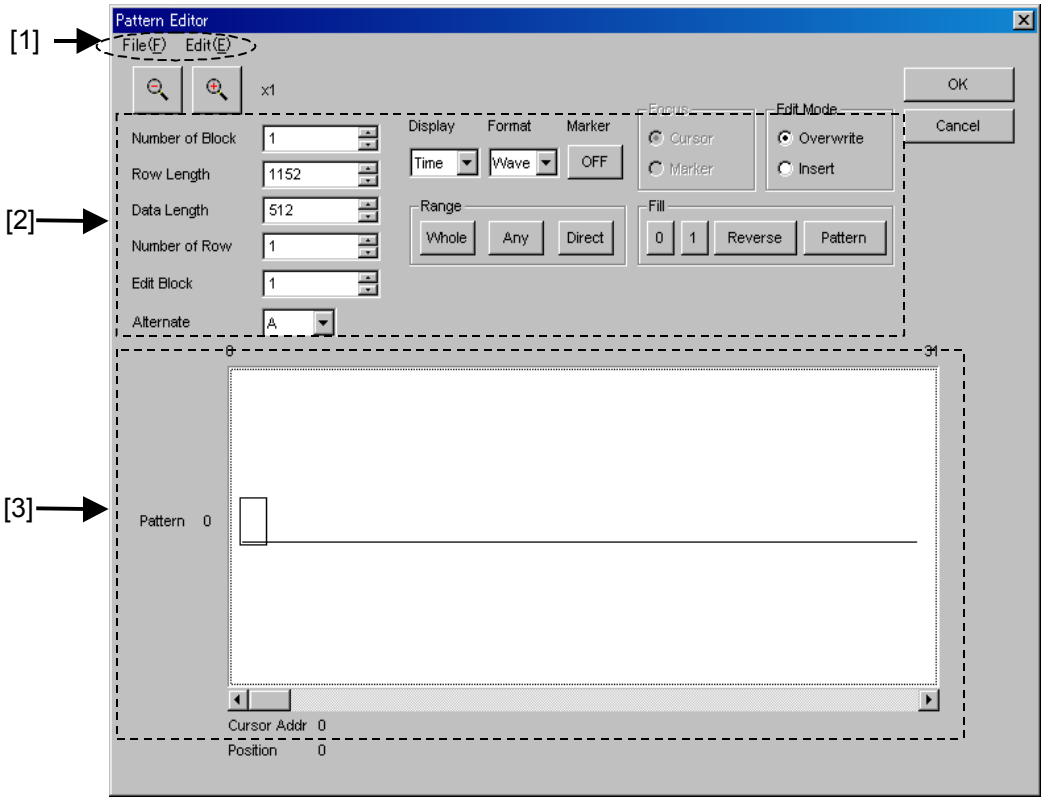


Figure 5.2.8.1-1 Pattern Editor dialog box

[1] Menu items on menu bar

Table 5.2.8.1-1 Menu bar configuration

Menu	Menu item	Description
File	Open	Opens a setting file saved in the binary pattern (Binary Pattern), binary text pattern (BIN Text Pattern), or hexadecimal text pattern (HEX Text Pattern) format. Refer to Section 5.2.8.11 "Compatibility with test pattern files of existing models" for details.
	Save	Saves a setting file in the binary pattern (Binary Pattern), binary text pattern (BIN Text Pattern), or hexadecimal text pattern (HEX Text Pattern) format. ***Note:*** The settings will not be read from the saved file if the file name is changed.
	Screen Copy	Prints a screen image. When configuring the print settings, select "Screen Copy" → "Setup" from the File menu on the MX18000A menu bar.
Edit	Undo	Restores the previous state.
	Cut	Cuts the pattern selected in the Pattern View area and transfers it onto the clipboard. The area that has been cut out becomes 0.
	Copy	Copies the pattern selected in the Pattern View area into the internal memory.
	Paste	Pastes the pattern copied in the internal memory to the cursor position.
	Jump	Moves the cursor to a specified address or pattern.
	Head	Moves the cursor to the start of the editing pattern.
	Tail	Moves the cursor to the end of the editing pattern.
	Marker	Moves the cursor to a position specified by the marker when set to ON.
	Address	Opens the Input Address setup dialog box. The cursor can be moved to the specified address position.
	Pattern	Opens the Input Pattern setup dialog box. Specifies a pattern string to search by binary digits, and a pattern to be masked by an "x". If a pattern matching the search condition is found in the editing pattern, the cursor moves to that position. Both forward search and backward search are supported. The search pattern can be specified in the Input Pattern window. Click [Set All] to set all the bits to "1", and click [Reset ALL] to set all the bits to "0". Click [ALL X] to set all the bits to "Don't care". Select the search direction by clicking the [Forward] or [Backward] option button, and then click [OK].
	Forward Next	Searches for a pattern that matches the search pattern set in the Input Pattern setup dialog box in the forward direction. If a matching pattern is found, the cursor moves to that position.
	Backward Next	Searches for a pattern that matches the search pattern set in the Input Pattern setup dialog box in the backward direction. If a matching pattern is found, the cursor moves to that position.

Table 5.2.8.1-1 Menu bar configuration (Cont' d)

Menu	Menu item	Description
Edit (continued)	Line	Specifies the number of characters per line in the Pattern View area. This is enabled when the pattern setting item Display is set to "Table".

[2] Pattern setting items

Table 5.2.8.1-2 Pattern setting items

Setting item	Description
Display	Select the display format in the Patter View area from "Time" or "Table". Time: The Pattern View area is displayed based on the time axis. Table: The Pattern View area is displayed in a tabular format.
Format	Specify the pattern display format in the Pattern View area. When "Time" is selected for Display, "Wave" or "Bit" can be selected. Wave: The pattern is displayed by a waveform. Bit: The pattern is displayed by a bit string. Refer to Section 5.2.8.7 "Editing in Time display mode" for details. When "Table" is selected for Display, "Bin" or "Hex" can be selected. Bin: Binary Hex: Hexadecimal Refer to Section 5.2.8.8 "Editing in Table display mode" for details.
Marker	Click this button to place a marker in the Pattern View area. This is enabled when "Time" is selected for Display.
Focus	This is enabled when Marker is set to ON. Select whether to activate a marker or cursor in the Pattern View area.
Edit Mode	Specify the pattern editing method from "Overwrite" or "Insert". This must be specified in advance when executing Past from the Edit menu or when performing direct editing in the Pattern View area (except for the Fill setting area). Overwrite: The selected pattern is overwritten. Insert: The editing pattern is inserted into the position of the selected pattern. Note that Data Length is not changed when Insert is selected. The inserted pattern therefore exceeds the Data Length value, and becomes invalid.
Range	Specify the pattern editing range from "Whole", "Any", or "Direct". Whole: All editing patterns are selected as the editing range. Any: The Input Range setup dialog box (Refer to Figure 5.2.8.1-2) is displayed when this button is clicked. The editing range can be specified by an address. Direct: Select an arbitrary area by specifying addresses. Use the cursor to specify addresses. Refer to Section 5.2.8.9 "Editing area" for details.

Table 5.2.8.1-2 Pattern setting items (Cont'd)

Setting item	Description
Fill	Edits the pattern part highlighted by the cursor. 0: The highlighted part in the Pattern View area is set to "0". 1: The highlighted part in the Pattern View area is set to "1". Reverse: The highlighted part in the Pattern View area is logically inverted. Pattern: The Input Pattern setup dialog box (Refer to Figure 5.2.8.1-3) is displayed. The highlighted part in the Pattern View area can be edited in this dialog box. Length: Specify the number of edit bits from the start address of the highlighted part. Repeat: The edited pattern for which the highlighted address is set to the first is repeated for the number of times specified here. Set All: Sets all the bits selected by Length to "1". Reset All: Sets all the bits selected by Length to "0".
Zoom 	The waveform displayed in the Pattern View area can be enlarged or reduced by changing Zoom. The selectable scale is 1/8, 1/4, 1/2, 1, 2, 4, and 8. This is enabled only when "Time" is set for Display and "Wave" is set for Format.

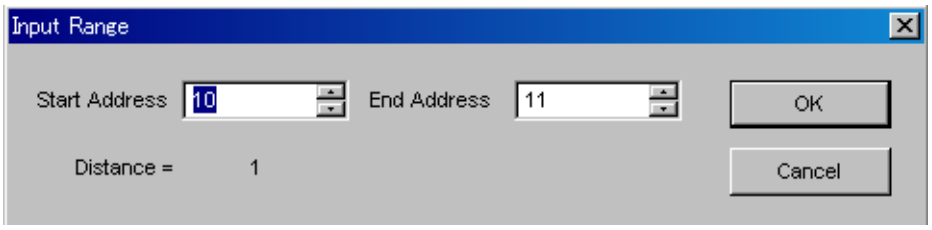


Figure 5.2.8.1-2 Input Range setup dialog box

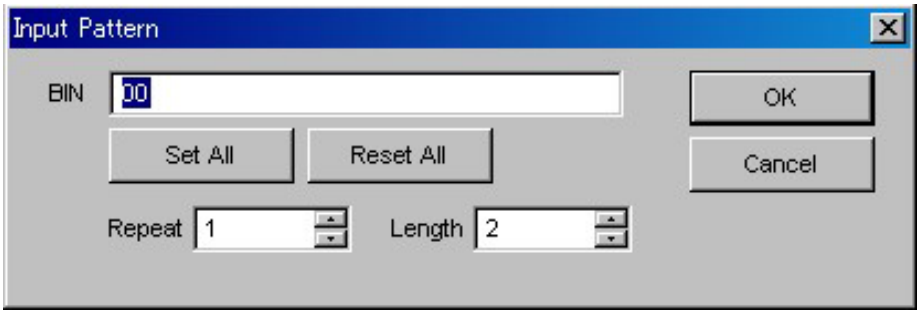


Figure 5.2.8.1-3 Input Pattern setup dialog box

[3] Pattern View area

The edited pattern is displayed in this area. Double-clicking a pattern enables the bit value to be changed. Note that the pattern cannot be edited by a mouse operation when Display is set to Table and Format is set to Hex.

5.2.8.2 Editing Data pattern

When [Edit] is clicked while Data is selected for the test pattern, the Pattern Editor dialog box shown in Figure 5.2.8.2-1 is displayed.

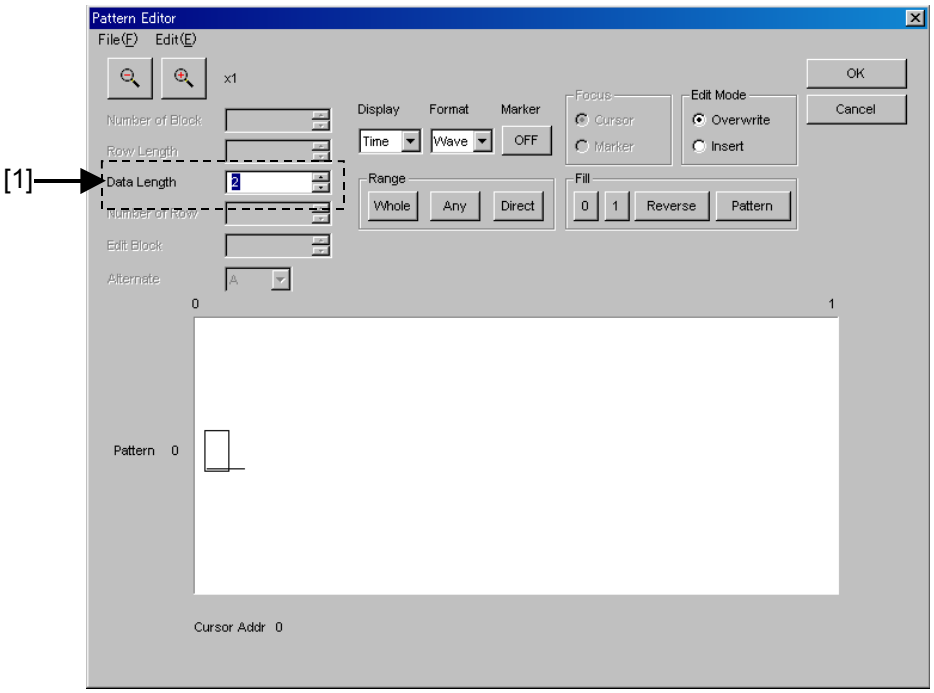


Figure 5.2.8.2-1 Pattern Editor dialog box for Data pattern

[1] Pattern setting item

Table 5.2.8.2-1 Pattern setting items (when Data is selected)

Setting item	Description
Data Length	Set the length of the Data pattern. The setting unit is one bit. 2 to 134,217,728 bits can be set, in 1-bit steps. In the case of 2 Ch Combination, 4 to 268,435,456 bits can be set, in 2-bit steps. In the case of 4 Ch Combination, 8 to 536,870,912 bits can be set, in 4-bit steps.

5.2.8.3 Editing Alternate patterns

When [Edit] is clicked while Alternate is selected for the test pattern, the Pattern Editor dialog box shown in Figure 5.2.8.3-1 is displayed.

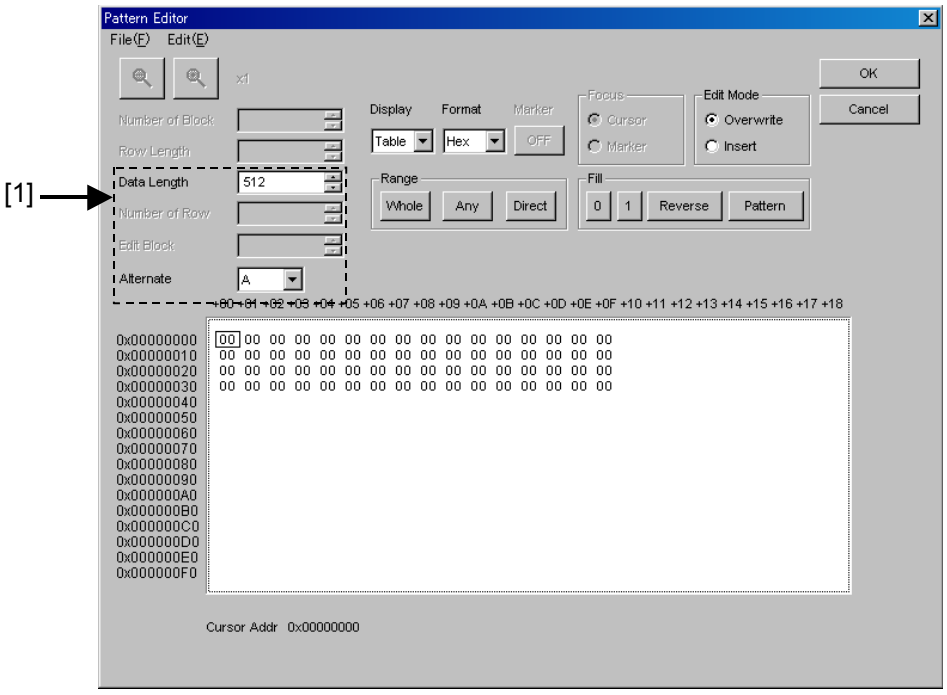


Figure 5.2.8.3-1 Pattern Editor dialog box for Alternate pattern

[1] Pattern setting item

Table 5.2.8.3-1 Pattern setting items (when Alternate is selected)

Setting item	Description
Data Length	Set the length of the Alternate pattern. The setting unit is one bit. 128 to 67,108,864 bits can be set for patterns A and B, in 128-bit steps.
Alternate	Specify whether alternate pattern A or B is to be edited.

5.2.8.4 Editing Mixed pattern

When [Edit] is clicked while Mixed is selected for the test pattern, the Pattern Editor dialog box shown in Figure 5.2.8.4-1 is displayed.

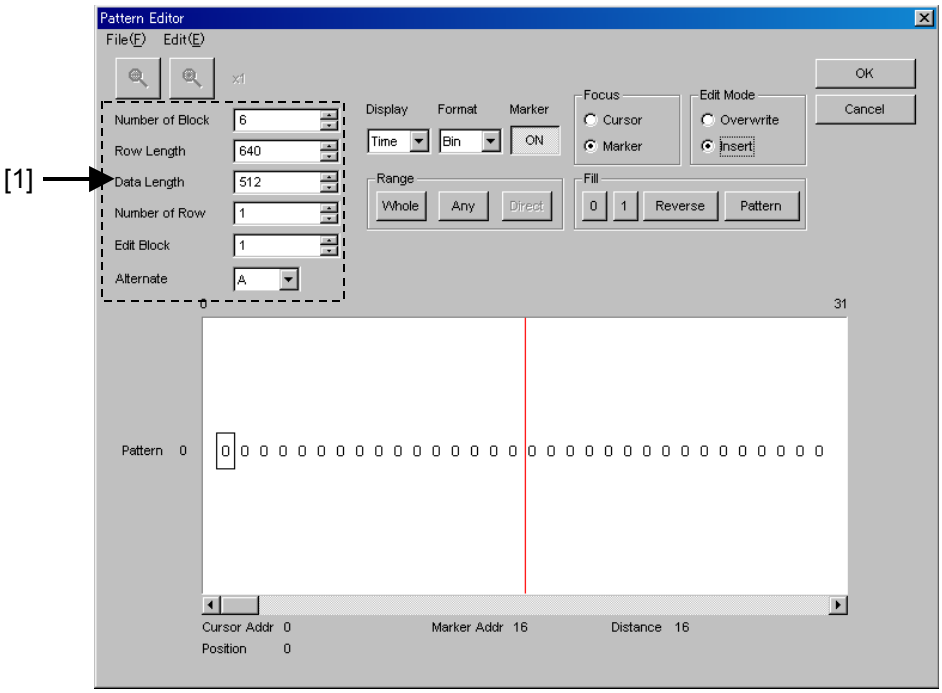


Figure 5.2.8.4-1 Pattern Editor dialog box for Mixed pattern

[1] Pattern setting items

Table 5.2.8.4-1 Pattern setting items (when Mixed is selected)

Setting item	Description
Number of Block	Set the number of blocks from 1 to 511, in 1-block steps.
Row Length	Set the row length. When Data is selected: Can be set from 768 to 2,281,701,376 bits, in 128-bit steps. In the case of 2 Ch Combination, set from 1,536 to 4,563,402,752 bits in 2-bit steps. In the case of 4 Ch Combination, set from 3,072 to 9,126,805,504 bits in 4-bit steps. When Alternate is selected: Can be set from 768 to 2,214,592,512 bits, in 128-bit steps.

Table 5.2.8.4-1 Pattern setting items (when Mixed is selected) (Cont'd)

Setting item	Description
Data Length	Set the pattern length. When Data is selected: Can be set from 512 to 134,217,728 bits, in 1-bit steps. In the case of 2 Ch Combination, set from 1,024 to 268,435,456 bits in 2-bit steps. In the case of 4 Ch Combination, set from 2,048 to 536,870,912 bits in 4-bit steps. When Alternate is selected: Can be set from 512 to 67,108,864 bits , in 128-bit steps.
Number of Row	Set the number of rows from 1 to 16, in 1-row steps.
Edit Block	Specify the number of blocks to be edited.
Alternate	Specify whether alternate pattern A or B is to be edited. This is enabled for the Mixed Alternate pattern.

Note:

The number of blocks and the number of rows are restricted as follows.

Number of blocks

1 to the smallest number among a to d, below, in 1-block steps

a) 511

b) INT (128 Mbits × x/(Number of rows × Data Length'))

where Data Length' is:

- When Data Length is indivisible by (128 × x)

=(INT(Data Length/(128 × x)) +1) × 128 × x

- When Data Length is divisible by (128 × x)

=Data Length

The maximum number of blocks fulfilling the following formula
applies:
Data Length' × Number of rows × Number of blocks ≤ 128 Mbits

c) INT((128 Mbits +2^{31}) × x/(Row Length × Number of rows))

where x is:

1 for Independent

2 for 2 Ch Combination

4 for 4 Ch Combination

d) (Row Length – Data Length) × Number of blocks ≥ 2^31(2147483648)

Number of Rows

1 to the smallest number among a to c, below, in 1-row steps

a) 16

b) INT(128 Mbit × x/Data Length')

where Data Length' is:

- When Data Length is indivisible by (128 × x)

=(INT(Data Length/(128 × x))+1)× 128 × x

- When Data Length is divisible by (128 × x)

=Data Length

The maximum number of rows fulfilling the following formula applies:
Data Length' × Number of rows × Number of blocks ≤ 128 Mbits

c) INT((128 Mbits +2^{31})× x/Row Length)

where x is;

1 for Independent

2 for 2 Ch Combination

4 for 4 Ch Combination

5.2.8.5 Editing Sequence pattern

When [Pattern Edit] is clicked while Sequence is selected for the test pattern, the Pattern Editor dialog box shown in Figure 5.2.8.5-1 is displayed.

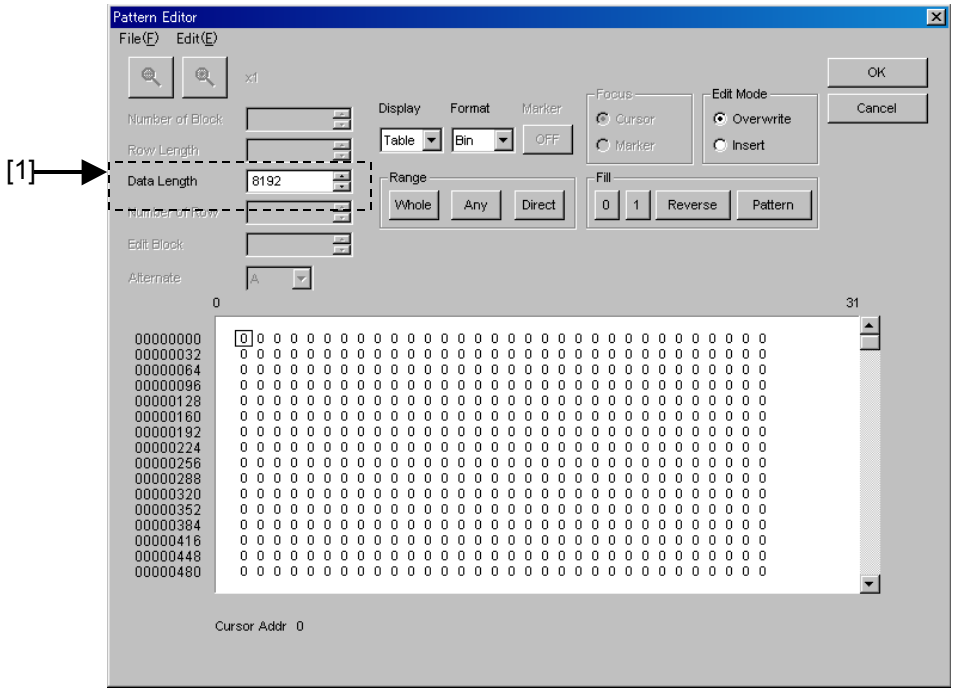


Figure 5.2.8.5-1 Pattern Editor dialog box for Sequence pattern

[1] Pattern setting items

Table 5.2.8.5-1 Pattern setting items (when Sequence is selected)

Setting item	Description
Data Length	Set the length of the Sequence pattern. The setting unit is one bit. The MU181020A can be set from 8,192 to 1,048,576 bits in 128-bit steps. The MU181020B can be set from 16,384 to 1,048,576 bits in 128-bit steps.

Note:

The [Pattern Editor] is enabled only when a block is set in the Sequence Pattern Setting dialog box.

5.2.8.6 Creating and editing test pattern

How to create and edit a test pattern in the Pattern Editor dialog box is described below.

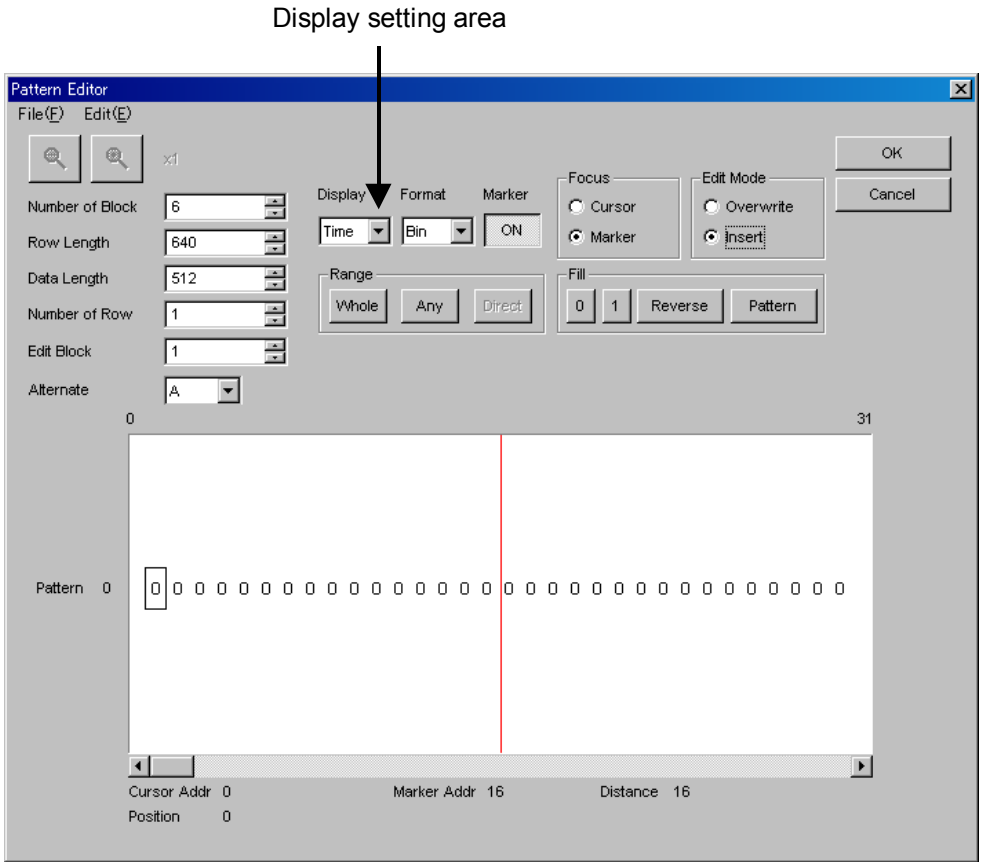


Figure 5.2.8.6-1 Display list box

1. Select the Pattern View area display format from the Display list box.

Table 5.2.8.6-1 Selection in Display setting area

Setting item	Description
Time	The test pattern is displayed and edited in a line with the horizontal time axis. The test pattern is displayed and can be edited with a waveform image or in binary.
Table	The test pattern is displayed and edited with a memory dump image. The test pattern is displayed and can be edited in binary or hexadecimal format.

2. For how to edit a test pattern in the Pattern Editor dialog box, Refer to the corresponding section according to the display mode, as follows:

When Time is selected:	Refer to Section 5.2.8.7 “Editing in Time display mode.”
When Table is selected:	Refer to Section 5.2.8.8 “Editing in Table display mode.”

5.2.8.7 Editing in Time display mode

How to create and edit a test pattern in the Time display mode is described below.

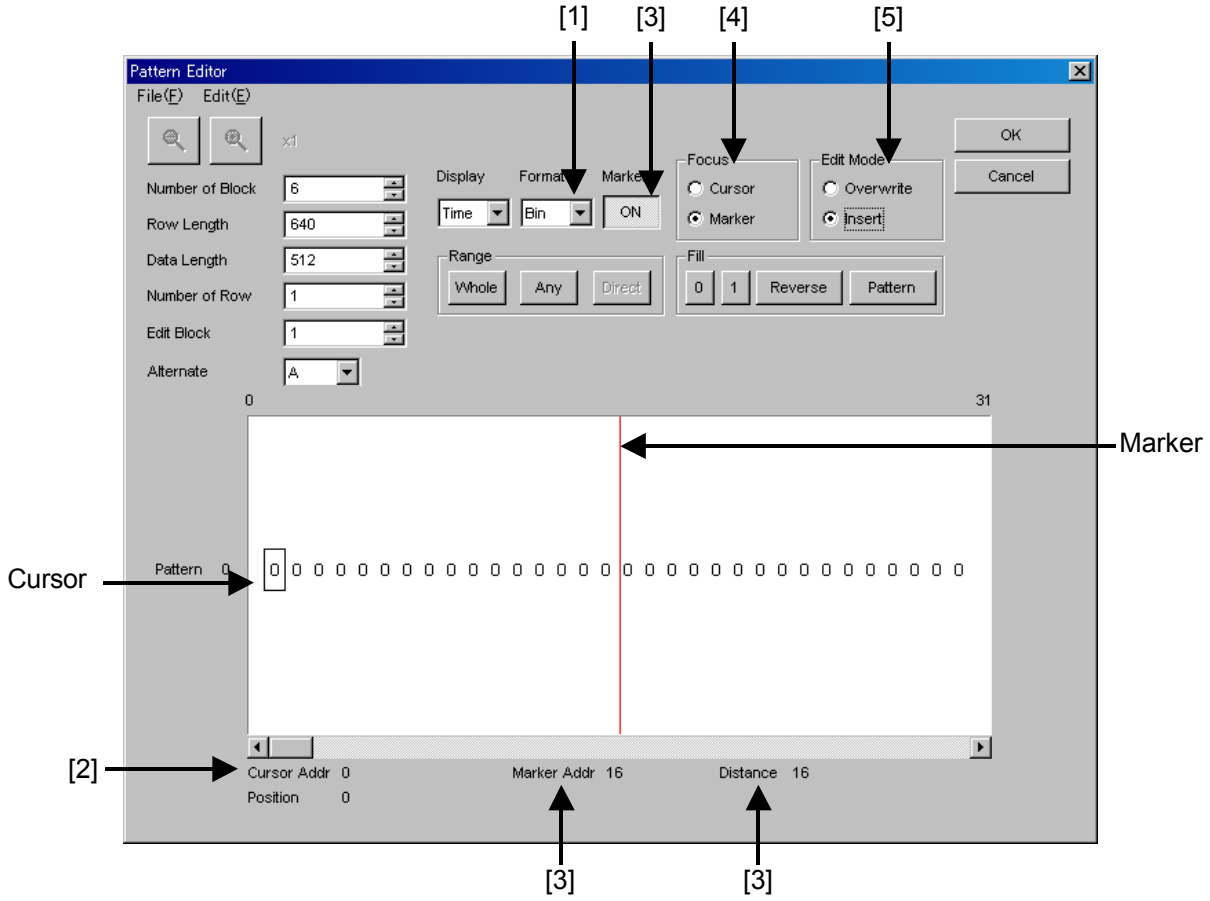


Figure 5.2.8.7-1 Editing in Time display mode

[1] Select the display format from the Format list box in the Pattern Editor dialog box.

Table 5.2.8.7-1 Display format setting

Setting item	Description
Wave	A test pattern is displayed and edited with a waveform image. The waveform image can be enlarged and reduced using the Zoom In and Zoom Out buttons.
Bin	A test pattern is displayed and edited in binary.

[2] The address of the cursor is displayed.

[3] Set marker display ON/OFF. The marker is displayed when the [Marker] is clicked and displayed as “ON”. The marker is not displayed when the button is clicked and displayed as “OFF”. The address of the marker and the distance between the cursor and marker are displayed in “Marker Addr” and “Distance”, respectively.

[4] Select the operation target. The cursor is operated when the Cursor radio button is selected, and the marker is operated when the Marker radio button is selected.

[5] Set the editing mode. Editing is performed in the insertion mode when the Insert radio button is selected, and is performed in the overwriting mode when the Overwrite radio button is selected.

5.2.8.8 Editing in Table display mode

How to create and edit a test pattern in the Table display mode is described below.

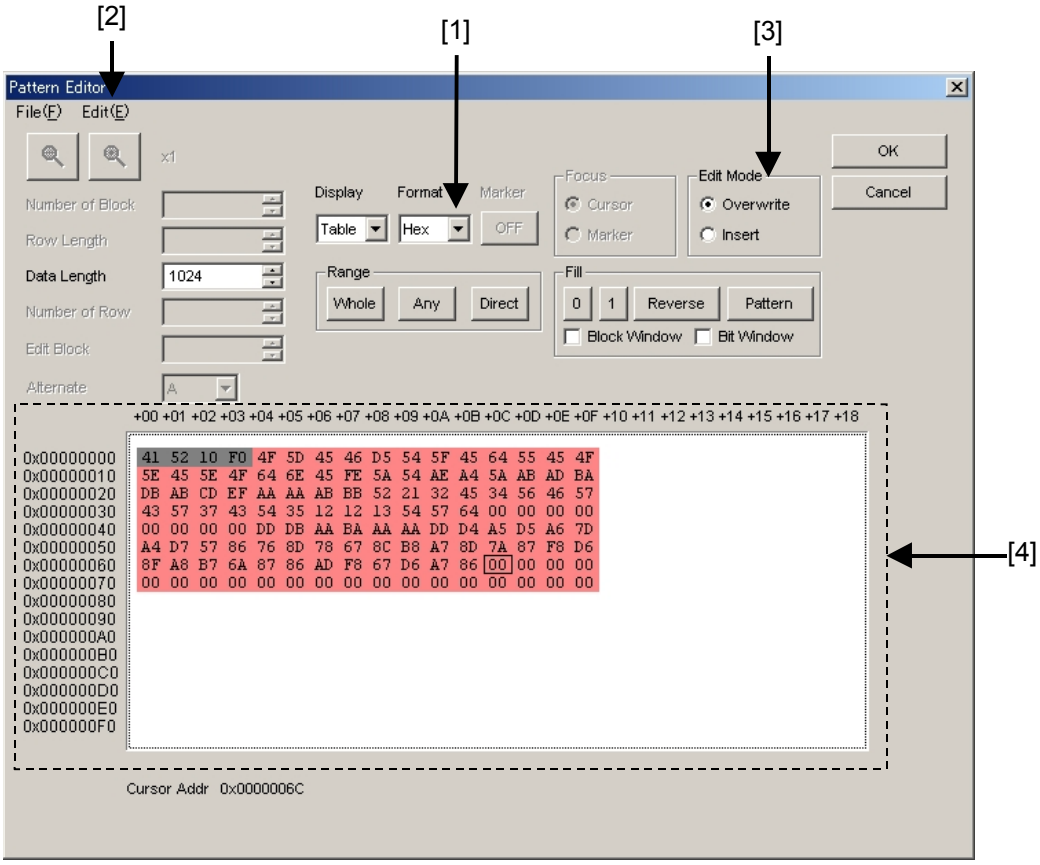


Figure 5.2.8.8-1 Editing in Table display mode

[1] Select the display format from the Format list box in the Pattern Editor dialog box.

Table 5.2.8.8-1 Display format setting

Setting item	Description
Bin	A test pattern is displayed and edited in binary.
Hex	A test pattern is displayed and edited in hexadecimal format.

[2] The amount of data to be displayed in one line can be changed. Select "Line" from the Edit menu to open the Line dialog box. Enter the number of bytes per line in the textbox, and then click [OK].

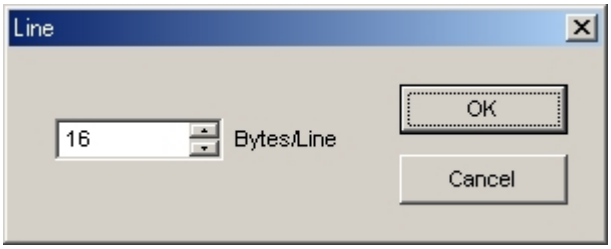


Figure 5.2.8.8-2 Line dialog box

[3] Set the editing mode. Editing is performed in the insertion mode when the Insert radio button is selected, and is performed in the overwriting mode when the Overwrite radio button is selected.

[4] Use the 0 and 1 keys for pattern input when the display format is binary. Use 0 to 9 and A to F keys when the display format is hexadecimal.

5.2.8.9 Editing area

In the Pattern Editor dialog box, batch editing is possible for an area by selecting it consisting of multiple bits. In this area, perform replace input using the Fill group box, or use Cut, Copy, and Paste editing commands.
The selection area setting procedure by using buttons in the Range group box is described below.

The function of each button is as follows:

Table 5.2.8.9-1 Area specification buttons

Button	Function
Whole	Specifies entire of the pattern as the selection area.
Any	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by entering values in the Input Range dialog box.
Direct	Sets an arbitrary area as the selection area by specifying addresses. The address is specified by using a cursor.

■ How to specify the selection area using the [Any] is as follows.

Figure 5.2.8.9-1 Input Range dialog box

1. Enter the start address of the selection area in the Start Address textbox.
2. Enter the end address of the selection area in the End Address textbox.
3. Click [OK] to set the specified area as the selection area. The selection area is highlighted in the Pattern Editor dialog box.

■ How to specify the selection area using the [Direct] is as follows.

1. Click [Direct]. The [Direct] is depressed and the Direct mode is entered. Note that pattern input and editing cannot be performed in the Direct mode.

2. Specify the start position of the selection area by double-clicking the desired position or by moving the cursor to that position and pressing the [Enter] key.
3. Specify the end position of the selection area. Display the desired position for the selection area by selecting "Jump" from the Edit menu, and then double-click the position or move the cursor to that position and press the [Enter] key.
4. The selection area is now completely set.

■ The selection area can also be specified by the following step.

1. Drag the mouse to select an area.

5.2.8.10 Inputting pattern

How to input a pattern by using the buttons in the Fill group box is described below. The function of each button is as follows:

Table 5.2.8.10-1 Fill button functions

Button	Function
0	Replaces the bit of the cursor position or the bits in the selection area to "0".
1	Replaces the bit of the cursor position or the bits in the selection area to "1".
Reverse	Inverts the bit of the cursor position or the bits in the selection area.
Pattern	Inputs an arbitrary pattern repeatedly.

■ How to input a pattern using the [Pattern] is as follows.

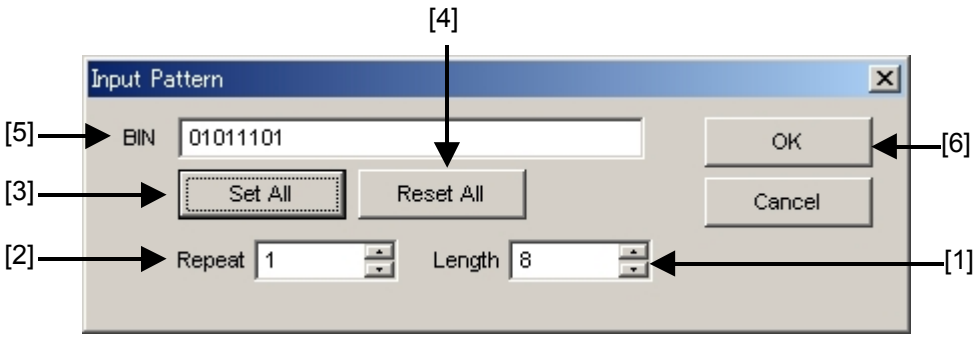


Figure 5.2.8.10-1 Input Pattern dialog box

[1] Enter the number of bits to be input.

[2] Enter the number of specified pattern repetition times.

[3] Click [Set ALL] to set all the bits to "1".

[4] Click [Reset ALL] to set all the bits to "0".

[5] Input a pattern into the BIN or HEX textbox.

[6] Click [OK] to input the pattern to the cursor position.

Note:

When the Input Pattern dialog box is displayed while the selection area is specified, a repetition of the specified pattern is applied to the selection area, regardless of the number of repetition times specified in the Repeat textbox.

5.2.8.11 Compatibility with test pattern files of existing models

Pattern files (.PTN) created for the following existing models can be loaded into the Pattern Editor dialog box of the MU181020A.

- MP1632C Digital Data Analyzer
- MP1761A/B/C Pulse Pattern Generator
- MP1762A/C/D Error Detector
- MP1775A Pulse Pattern Generator
- MP1776A Error Detector

5.3 Adding Errors

An error can be added to output data by configuring the error occurrence settings in the Error Addition tab window.

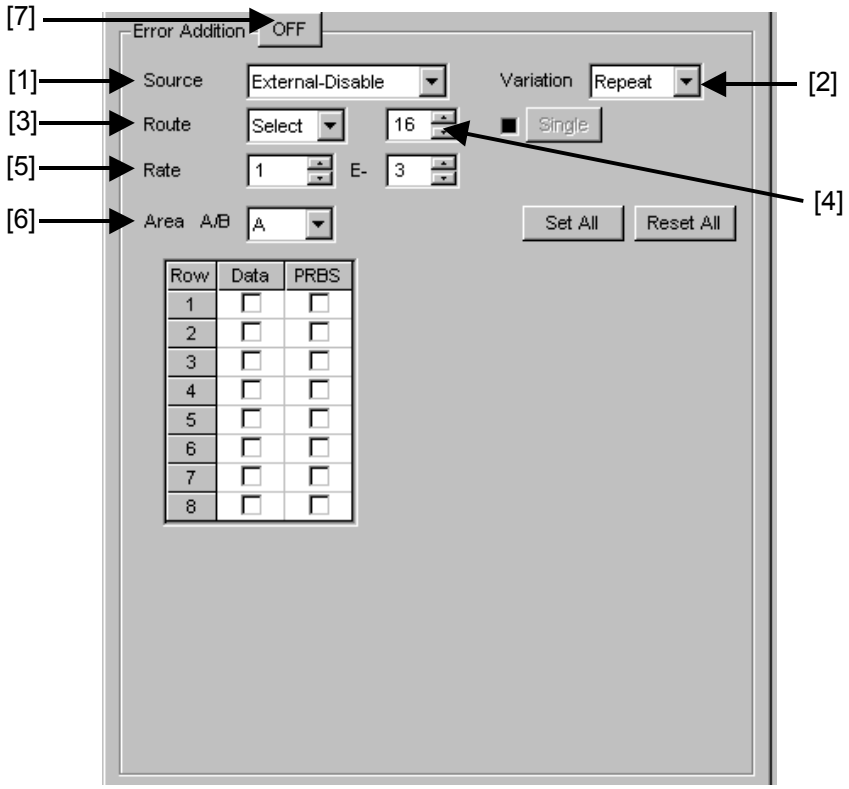


Figure 5.3-1 Error Addition tab window

[1] Selecting error adding source

Select the method for generating the timing to add a specified bit error to the test pattern.

Table 5.3-1 Error addition source setting

Setting item	Description
Internal	The error addition timing is generated by the internal circuit.
External-Trigger	The error addition timing is generated in synchronization with the trigger edge of the external signal input from the Auxiliary Input connector. This cannot be set when Error-Injection is not set for AUX Input in the Misc tab window.
External-Disable	The error addition timing is generated by the internal circuit, but an error is not added when the external signal input from the Auxiliary Input connector is low. This cannot be set when Error-Injection is not set for AUX Input in the Misc tab window.

[2] When “Internal” or “External-Disable” is selected, select the error addition variation. Select the error insertion method when adding an error (internal Gating).

Table 5.3-2 Error insertion method setting

Setting item	Description
Repeat	An error is continuously inserted.
Single	An error is inserted once when the button is clicked. Note that the following restrictions apply. (a) Enabled only when “Internal” or “External-Disable” is selected from the Source list box. (b) Disabled when “External-Trigger” is selected.

[3] Select the method for inserting an error addition route.

Table 5.3-3 Error addition route setting

Setting item	Description
Scan	A route for which a 1/1 signal is demultiplexed by 32 is changed each time an error is inserted.
Select	An error is inserted to the specified route.

[4] Specify a route to generate a 1-bit error for the test pattern. The route can be specified from 1 to 32, in single steps.

Note that the following restrictions apply.

(a) This setting is valid even when the error addition function is set to OFF.

(b) This setting is invalid when Scan is selected in the Route list box.

[5] Select the bit error rate to generate a 1-bit error for the test pattern.

xE–n: x can be set to 1 to 9, in single steps.
n can be set to 2 to 12, in single steps.

Note that the following restrictions apply.

(a) The setting is valid even when the error addition function is set to OFF.

(b) This setting is invalid when the error addition variation setting is set to Single.

(c) This setting is invalid when the error addition source is set to External-Trigger.

(d) n can be set to 3 to 12 in the case of Combination.

(e) x can only be set to 1 when n is set to 2.

[6] For the Mixed pattern, select the block (Data/PRBS and Block No.) where a bit error is to be inserted.

Area A/B: The setting range varies depending on the following conditions.

(a) For Mixed patterns:
Any combination of areas in the specified blocks can be selected.
Note, however, that this setting commonly applies to the blocks. In the case of the Mixed Alternate pattern, the area specification can be set separately for pattern A, pattern B, and patterns A and B.

(b) For Alternate patterns:
Only A, Only B, and A & B can be selected.

(c) For Sequence patterns:
An arbitrary block can be selected.

[7] Enables/disables generating a bit error for the test pattern.

ON: Enables the error addition function.

OFF: Disables the error addition function.

Note that this setting effects all error addition functions. When set to OFF, bit error addition triggered by an external error signal is also disabled.

5.4 Misc Function

The settings of the signal generating method, synchronized output, and auxiliary input/output can be configured.
Click the [Misc] tab on the ED module operation window to display the Misc tab window.

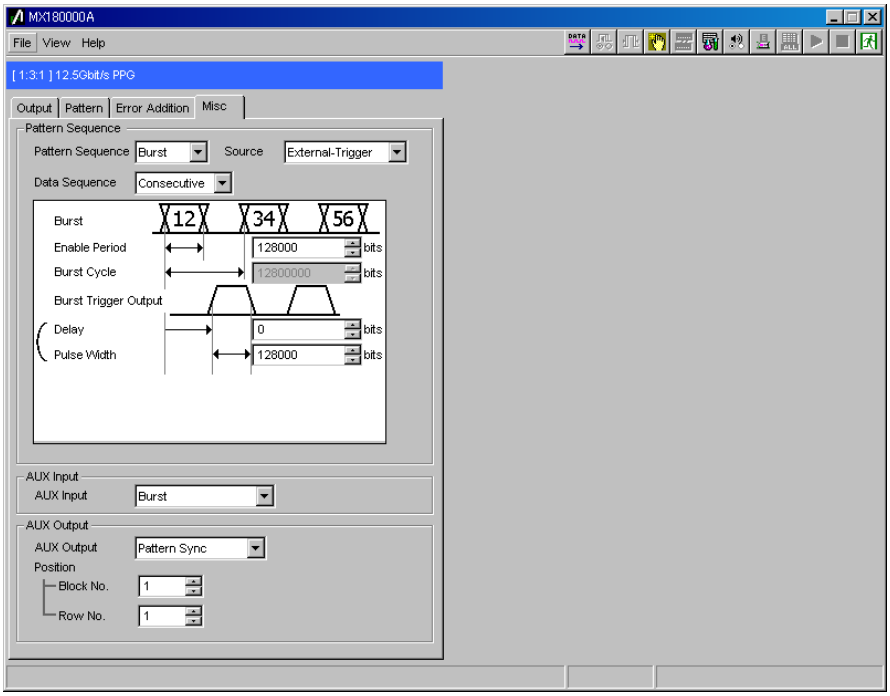


Figure 5.4-1 Misc tab window

Table 5.4-1 Setting items

Setting area	Description
Pattern Sequence	Set the test pattern generating method.
AUX Output	Configure the settings for the auxiliary output function.
AUX Input	Configure the settings for the auxiliary input function.

5.4.1 Setting pattern sequence

Select the signal generating method.

Figure 5.4.1-1 Selecting sequence

Table 5.4.1-1 Pattern sequence setting

Selection item	Description
Repeat	Select when transmitting the test pattern Repeat data. Mainly used for electric device evaluation.
Burst	Select when transmitting the test pattern Burst data. Mainly used for long-distance optical transmission tests such as an optical circulating loop test, and packet communications evaluation. The target test patterns are PRBS, Zero-Substitution, Data, and Mixed (Data).

5.4.1.1 Setting Repeat pattern

Select "Repeat" from the Pattern Sequence list box to transmit the test pattern Repeat data.

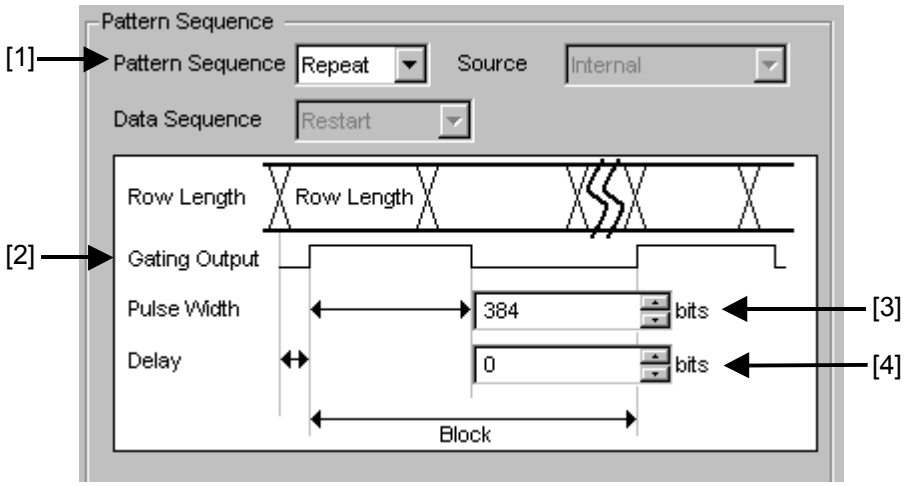


Figure 5.4.1.1-1 Setting items for Repeat pattern sequence

[1] Select "Repeat" from the Pattern Sequence list box, and generate continuous test patterns and data signals.

[2] Configure the settings related to the synchronization signal that is output from the Gating Output connector. The period of data signal synchronization output is calculated from the following expression, according to the signal type.

Table 5.4.1.1-1 Gating output setting range

Periodic Signal	Setting Range
PRBS, Data, Zero Substitution	(Least common multiple of Pattern length and 64) In the case of 2 Ch Combination Least common multiple of Pattern Length and 128 In the case of 4 Ch Combination Least common multiple of Pattern Length and 256
Mixed	(Row length × Number of Rows × Block count)
Alternate	(Pattern length of pattern A or B)
Sequence	Pattern length of the specified block

[3] In the Pulse Width textbox, specify the high level pulse width of the synchronization signal that is output from the Gating Output connector. The pulse width should be a multiple of 16. The Data Length setting value is calculated from the following expression, according to the signal type.

Table 5.4.1.1-2 Pulse width setting range

Periodic Signal	Setting Range [Step16 bit]
PRBS, Data, Zero Substitution, Alternate	0 to (Least common multiple of Pattern length and 64) – 64 (The maximum settable number is 68,719,476,672) In the case of 2 Ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution) is 0 to (Least common multiple of Pattern Length and 128) – 128 and the setting step becomes 32 bits. (The maximum settable number is 139,438,953,344) In the case of 4 Ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution) is 0 to (Least common multiple of Pattern Length and 256) –256 and the setting step becomes 64 bits. (The maximum settable number is 274,877,906,,688)
Mixed	0 to (Row length × Number of Rows × Block count) – 64 In the case of 2 Ch Combination is 0 to (Row length × Number of rows × Block count) – 128, and the setting step becomes 32 bits. In the case of 4 Ch Combination is 0 to (Row length × Number of rows × Block count) –256, and the setting step becomes 64 bits.
Sequence	0 to 64 (without block) 0 to (Pattern length of the specified block) – 64 (with block)

*: At Independent, when the pattern length is 128 bits or less, specify the length as an integer multiple so that it becomes 129 bits or more.
At 2 Ch Combination, when the pattern length is 256 bits or less, specify the length as an integer multiple so that it becomes 257 bits or more.
At 4 Ch Combination, when the pattern length is 512 bits or less, specify the length as an integer multiple so that it becomes 513 bits or more.

[4] In the Delay textbox, specify how many bits the data output is delayed from the beginning of the data pattern. The delay should be a multiple of 16. The delay is calculated from the following expression, according to the signal type.

Table 5.4.1.1-3 Delay setting range

Periodic Signal	Setting Range [Step16 bit]
PRBS, Data, Zero Substitution, Alternate	0 to (Least common multiple of Pattern length and 64) – 64(The maximum settable number is 68,719,476,672) In the case of 2 Ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution), is 0 to (Least common multiple of Pattern Length and 128) – 128 and the setting step becomes 32 bits. (The maximum settable number is 139,438,953,344) In the case of 4 Ch Combination (the target test patterns are PRBS, Data, and Zero-Substitution), is 0 to (Least common multiple of Pattern Length and 256) –256 and the setting step becomes 64 bits. (The maximum settable number is 274,877,906,688)
Mixed	0 to (Row length × Number of Rows × Block count) – 64 In the case of 2 Ch Combination is 0 to (Row length × Number of rows × Block count) – 128, and the setting step becomes 32 bits. In the case of 4 Ch Combination is 0 to (Row length × Number of rows × Block count) –256, and the setting step becomes 64 bits.
Sequence	0 to (Pattern length of the specified block) – 64 (with block)

*: At Independent, when the pattern length is 127 bits or less, specify the length as an integer multiple so that it becomes 128 bits or more.
At 2 Ch Combination, when the pattern length is 255 bits or less, specify the length as an integer multiple so that it becomes 256 bits or more.
At 4 Ch Combination, when the pattern length is 511 bits or less, specify the length as an integer multiple so that it becomes 512 bits or more.

Note:

In regard to Sequence, the specified block is determined by the setting in the Position - Block No. text box in the AUX Output area when “Pattern Sync” is selected from the AUX Output list box.

5.4.1.2 Setting Burst pattern

Select "Burst" from the Pattern Sequence list box to transmit the test pattern Burst data.

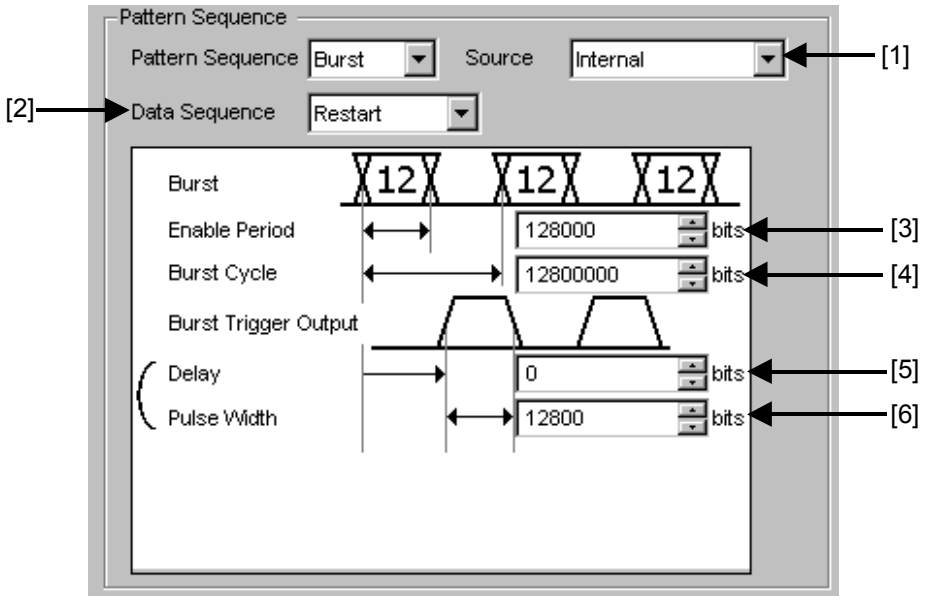


Figure 5.4.1.2-1 Setting items for Burst pattern sequence

Note:

The Burst Trigger Output signal is output from the Gating Output connector.

[1] Select the timing to generate test patterns with the Burst signal.

Table 5.4.1.2-1 Burst setting items

Setting item	Description
Internal	The Burst signal occurrence timing is generated by the internal circuit.
External-Trigger	The Burst signal occurrence period is generated based on the gate signal input from the external connector. Burst pattern generation starts at the rising edge of the input gate signal.
External-Disable	The Burst signal occurrence period is generated based on the gate signal input from the external connector. The Burst data is generated when the gate signal is high, and is not generated when the gate signal is low.

[2] Specify the burst pattern generating sequence.

Table 5.4.1.2-2 Burst pattern generation sequence setting

Setting item	Description
Restart	The specified test pattern is restarted from the beginning each time a Burst data signal occurs.
Consecutive	The specified test pattern is continuously output between Burst data signals.
Continuous	The specified test pattern is continuously output, and outputs other than the Burst occurrence timing are masked.

[3] When External-Trigger or Internal is selected from the Source list box ([1] in Figure 5.4.1.2-1), set the continuous signal generation period for the Burst cycle of the test pattern to be input to the AUX Input connector, by entering the number of bits in the Enabled Period text box. The setting ranges for Enable Period are shown in Table 5.4.1.2-3.

[4] When Internal is selected from the Source list box ([1] in Figure 5.4.1.2-1), set the Burst cycle (one cycle of the Burst signal of the test pattern to be input) by entering the number of bits in the Burst Cycle text box. The setting ranges for Burst Cycle are shown in Table 5.4.1.2-3.

Table 5.4.1.2-3 Setting ranges for Enable Periods and Burst Cycles

No. of Slot Combinations	Enable Period(bit)	Burst Cycle(bit)	Setting Steps (bit)
1	When Internal is set: 640 to 2,147,483,136	1,280 to 2,147,483,648	128
	When External-Trigger is set: 640 to 2,147,483,648		
2	When Internal is set: 1,280 to 4,294,966,272	2,560 to 4,294,966,296	256
	When External-Trigger is set: 1,280 to 4,294,966,296		
4	When Internal is set: 2,560 to 8,589,932,544	5,120 to 8,589,934,592	512
	When External-Trigger is set: 2,560 to 8,589,932,592		

Note:

A Disable period of at least 512 bits is required between Burst Cycle and Enable Period. The Disable period is doubled at 2 Ch Combination and quadrupled at 4 Ch Combination.

[5], [6] Set the Burst timing signal that is output from the Burst Trigger Output connector.

Delay: Specify how many bits the data output is delayed from the beginning of the Burst data pattern. The setting range is between 0 and the setting value of Burst Cycle, in 16-bit units.

Pulse Width: Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector.

The setting ranges for Delay and Pulse Width are shown in Table 5.4.1.2-4.

Table 5.4.1.2-4 Setting ranges for Delay and Pulse Width

No. of Slot Combinations	Delay (bits)	Pulse Width (bits)	Setting Steps (bits)
1	0 to Burst Cycle – 64	0 to Burst Cycle – 64	16
2	0 to Burst cycle－128	0 to Burst cycle－128	32
4	0 to (Burst Cycle) – 256	0 to (Burst Cycle) – 256	64

5.4.2 Setting AUX Output

The output settings of auxiliary signals, such as the synchronization signal, can be configured.

5.4.2.1 Setting 1/N Clock

A divided clock can be generated in synchronization with a generation pattern.

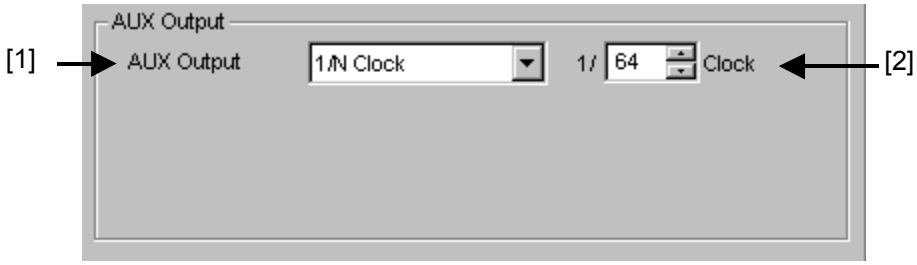


Figure 5.4.2.1-1 Setting items for AUX Output Clock

[1] When "1/N Clock" is selected from the AUX Output list box, a clock can be output from the AUX Output connector in synchronization with the test pattern.

[2] The frequency dividing ratio for the synchronization clock can be set. The setting range for the setting frequency dividing ratio (N) varies depending on the options installed, as follows.

Table 5.4.2.1-1 Synchronization clock dividing ratio setting

Setting Item	Synchronization Clock	Setting Frequency Dividing Ratio (N)
MU181020A-001	9.8 to 12.5 Gbit/s	2, 4, 8, 9, 10, 11, ..., 510, 511
1/8 Mode	1.225 to 1.5625 Gbit/s	1, 2, 4, 8, 9, 11, ..., 62, 63
1/4 Mode	2.45 to 3.125 Gbit/s	1, 2, 4, 8, 9, 11, ..., 126, 127
1/2 Mode	4.9 to 6.25 Gbit/s	1, 2, 4, 8, 9, 11, ..., 254, 256
MU181020A-002	0.1 to 12.5 Gbit/s	2, 4, 8, 9, 10, 11, ..., 510, 511
MU181020B-002	0.1 to 14 Gbit/s	2, 4, 8, 9, 10, 11, ..., 510, 511
MU181020B-003	0.1 to 14.05 Gbit/s	2, 4, 8, 9, 10, 11, ..., 510, 511

5.4.2.2 Setting Pattern Sync

A timing signal can be generated in synchronization with the test pattern period.

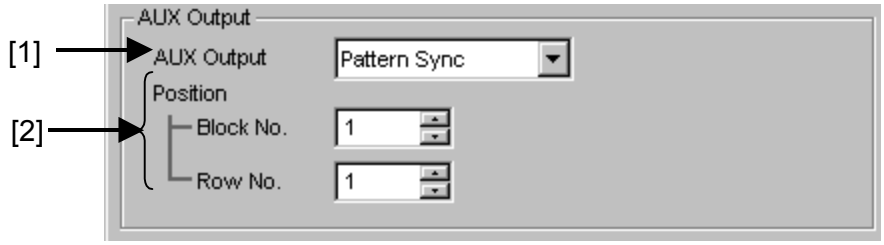


Figure 5.4.2.2-1 Setting items for AUX Output Pattern Sync

[1] When "Pattern Sync" is selected from the AUX Output list box, a pulse signal can be output from the AUX Output connector in synchronization with the set data pattern period.

[2] The synchronization signal pulse generation position can be set. The setting method varies depending on the test pattern.

Table 5.4.2.2-1 Synchronization signal pulse generation position setting

Test pattern	Description
PRBS	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps. The maximum settable number is 68,719,476,657 In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 128) -160}, in 32-bit steps. The maximum settable number is 137,438,953,312 In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) -319}, in 64-bit steps. The maximum settable number is 274,877,906,625
Zero-Substitution	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps. The maximum settable number is 68,719,476,657 In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 128) -160}, in 32-bit steps. The maximum settable number is 137,438,953,312 In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) -319}, in 64-bit steps. The maximum settable number is 274,877,906,625

Table 5.4.2.2-1 Synchronization signal pulse generation position setting (Cont'd)

Test pattern	Description
Data	A signal pulse is generated in a pattern period. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps. The maximum settable number is 68,719,476,957 In the case of 2 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 128) -160}, in 32-bit steps. The maximum settable number is 137,438,953,312 In the case of 4 Ch Combination: 1 to {(Least common multiple of Pattern Length* and 256) -319}, in 64-bit steps. The maximum settable number is 274,877,906,625
Alternate	A signal pulse is generated in one specified pattern period, A or B. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps.
Mixed (Data)	A signal pulse is generated during the entire block generation pattern period. The pulse position can be specified by the positions of Block and Row.
Mixed (Alternate)	A signal pulse is generated for the specified block number and alternate pattern (A or B). The pulse position can be specified in the position of the specified row.
Sequence	A signal pulse is generated in the specified block number. The pulse position can be specified within the range below, starting from the beginning of the pattern. 1 to {(Least common multiple of Pattern Length* and 64) -79}, in 16-bit steps.

*: At Independent, when the pattern length is 128 bits or less, specify the length as an integer multiple so that it becomes 129 bits or more.
At 2 Ch Combination, when the pattern length is 256 bits or less, specify the length as an integer multiple so that it becomes 257 bits or more.
At 4 Ch Combination, when the pattern length is 512 bits or less, specify the length as an integer multiple so that it becomes 513 bits or more.

5.4.2.3 Setting Burst Output2

When Burst is selected from the Pattern Sequence list box, a timing signal similar to the Burst Trigger Output signal can be output from the AUX Output connector.

Table 5.4.2.3-1 Burst Output2 setting

Setting item	Description
Delay	Specify how many bits the data output is delayed from the beginning of the Burst data pattern. The setting range is similar to Table 5.4.1.2-4 Setting ranges for Delay and Pulse Width.
Pulse Width	Specify the high level pulse width of the synchronization signal that is output from the Burst Trigger Output connector. The setting range is similar to Table 5.4.1.2-4 Setting ranges for Delay and Pulse Width.

5.4.3 Setting AUX Input

Use the AUX Input connector when inserting an error based on the externally-generated timing signal. This section describes the function that uses the AUX Input connector.

Figure 5.4.3-1 Setting item for AUX Input

Table 5.4.3-1 Setting items

Setting item	Description
Error Injection	Select when inserting an error based on the timing of an external signal. This is used when "External-Trigger" or "External-Disable" is selected from the Source list box in the Error Addition tab window (Refer to Section 5.3 "Adding Errors" for details). In the case of Combination, be sure to use AUX Input in Slot 1. Slots 2 to 4 cannot be used. In this case, an error is added in 4-bit units.
Alternate Control	Select when the generation pattern includes alternate patterns and patterns A and B should be switched (Refer to Sections 5.2.5 "Setting Alternate pattern" and 5.2.6.2 "Setting Mixed Alternate pattern" for details).
Sequence Control	Select when Sequence is selected for the generation pattern and External Trigger is specified for the state transition timing (Refer to Sections 5.2.7 "Setting Sequence pattern" for details).
Burst	Select when Burst is selected from the Pattern Sequence list box, and External-Trigger or External Enable is selected from the Source list box (Refer to Section 5.4.1.2 "Setting Burst pattern" for details). In the case of Combination, be sure to use AUX Input in Slot 1. Slots 2 to 4 cannot be used.
Unit Sync	Select when the Unit Sync is set to ON. (Refer to Appendix E "Preparing to Use Unit Sync Function".)

5.5 Multi Channel Function

When multiple MU181020A modules are installed into the MP1800A/MT1810A, synchronized operation of multiple channels is enabled. Multi-channel functions include the Combination and Channel Synchronization functions.

Combination Function Types

(1) 4ch Combination: when four PPG/ED modules installed

(2) 25Gx2ch Combination: when four PPG/ED modules installed

(3) 2ch Combination: when two or more PPG/ED modules installed

Channel Synchronization Function Types

(1) 12.5G Channel Synchronization: when two or more PPG modules installed

(2) 25G Channel Synchronization: when four PPG modules installed

5.5.1 Combination Function

Using multiple MU181020A and/or MU181040A/B modules, the Multi-channel function synchronizes the generation and reception of patterns between modules, to evaluate 25 Gbit/s, 40 Gbit/s and PON applications. For the 25 Gbit/s MUX/DEMUX explained below, refer to the *Operation Manual of MU182020/21A* and *MU182040/41A*.

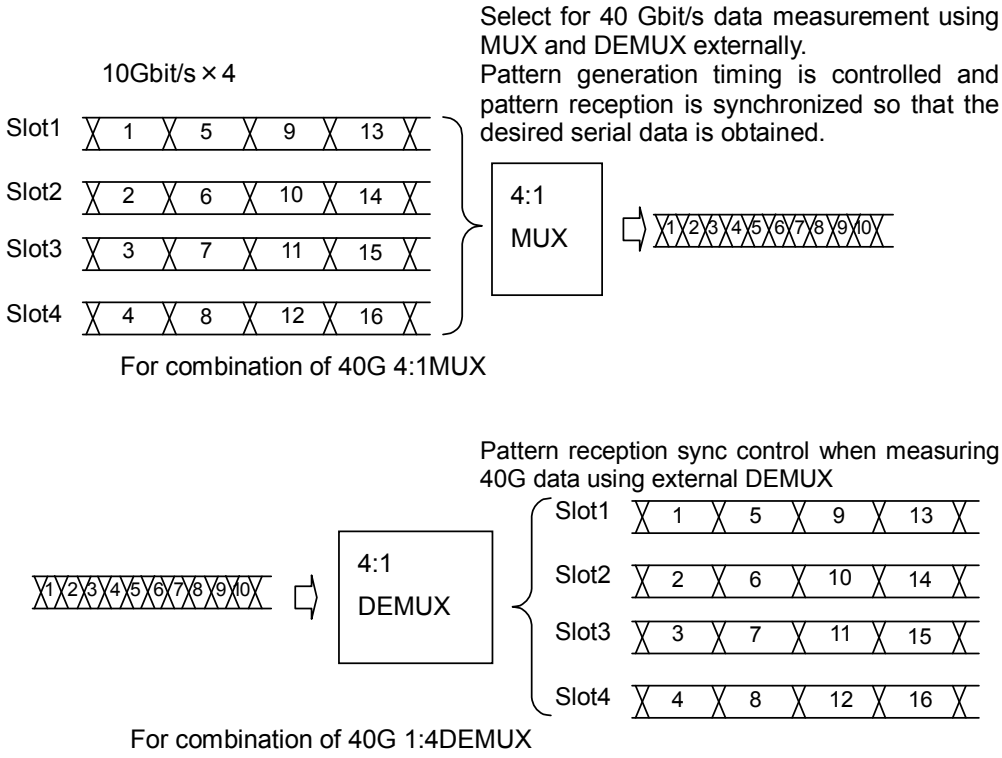


Figure 5.5.1-1 4ch Combination pattern generation/reception

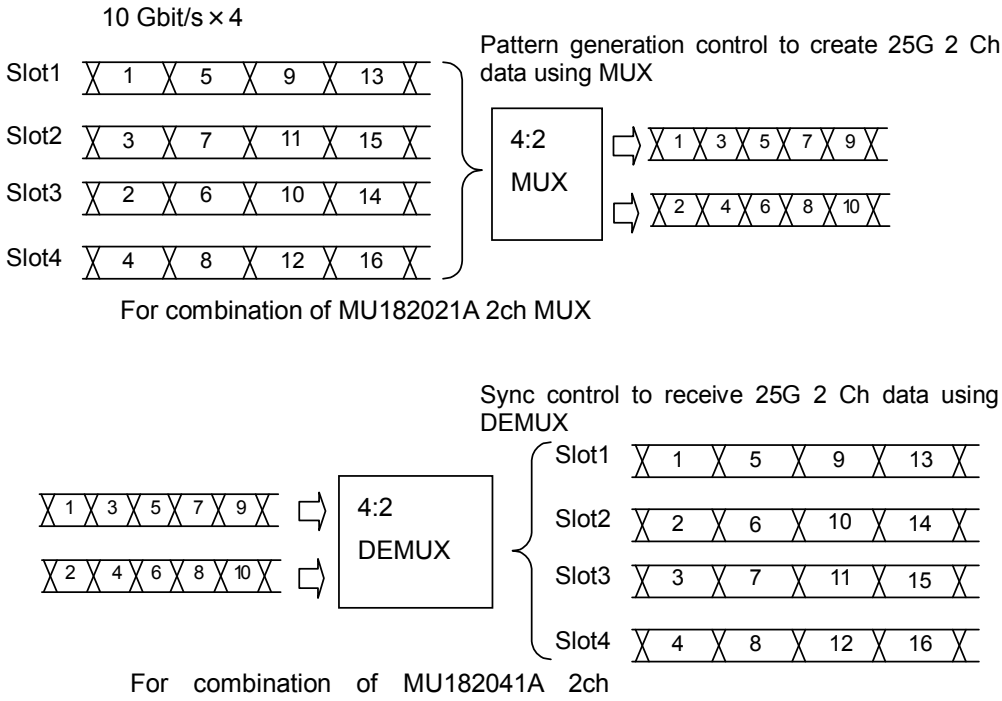


Figure 5.5.1-2 25Gx2ch Combination pattern generation/reception

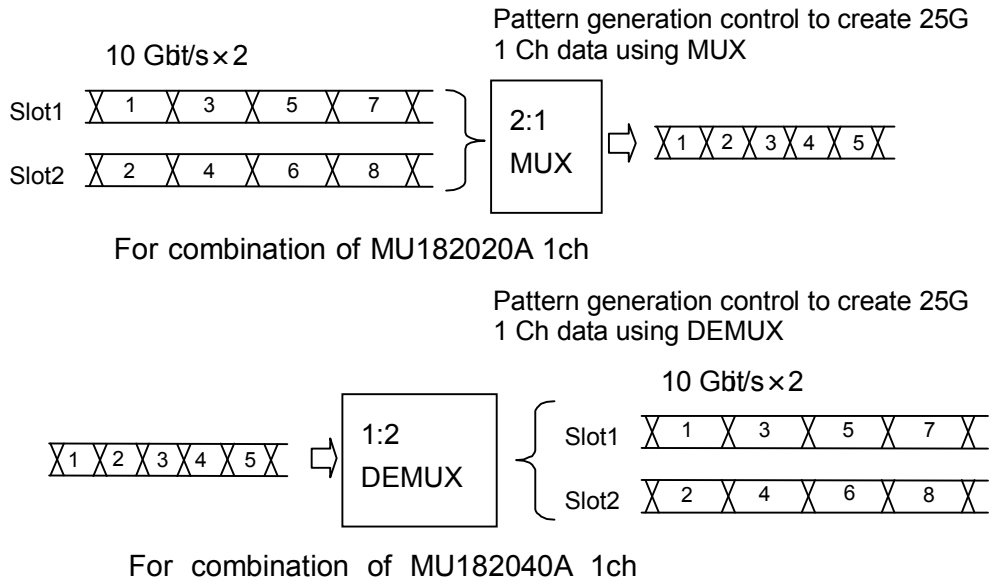


Figure 5.5.1-3 2ch Combination pattern generation/reception

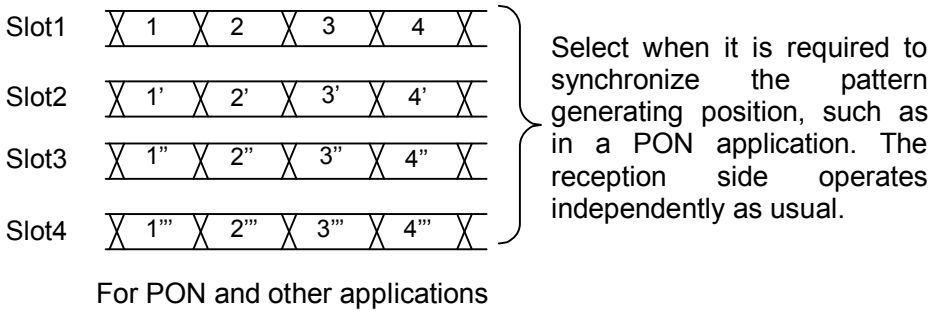


Figure 5.5.1-4 Channel Synchronization pattern generation/reception

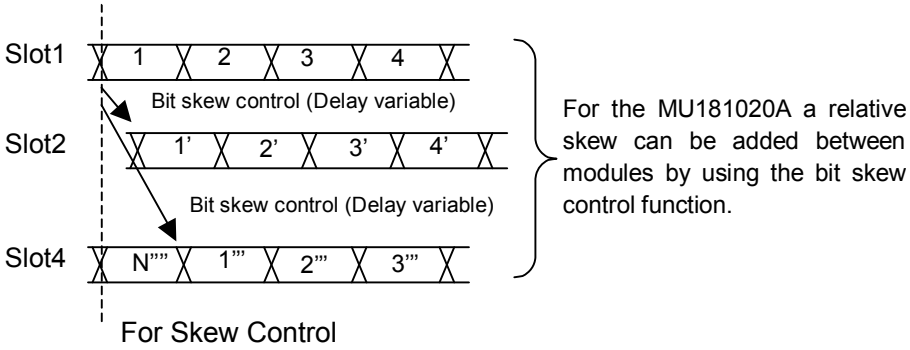


Figure 5.5.1-5 Skew Channel Synchronization Pattern

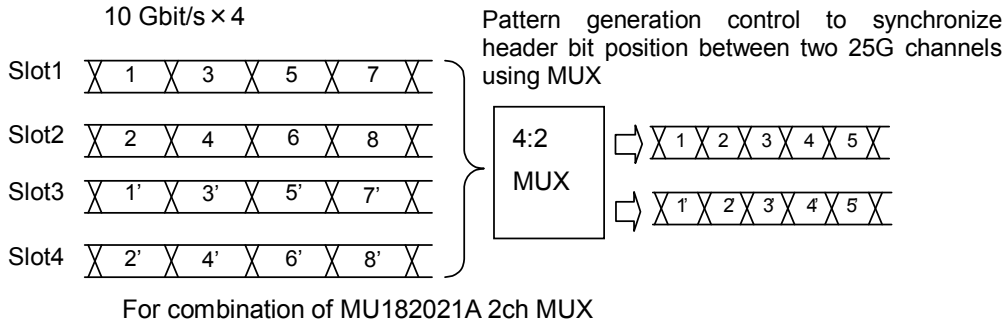


Figure 5.5.1-6 25G Channel Synchronization pattern generation/reception

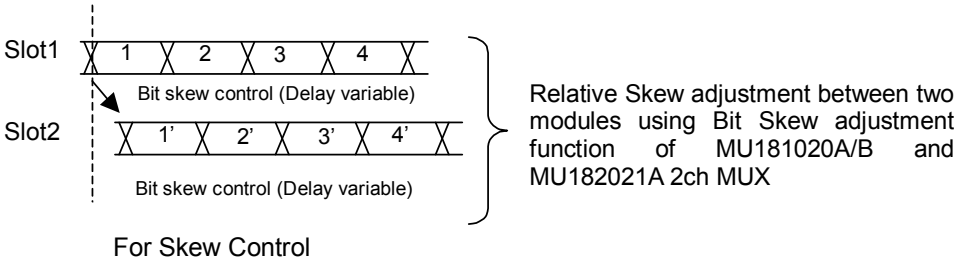


Figure 5.5.1-7 25Gx2ch Combination pattern generation/reception

5.5.2 Combination Setting

To use the Multi-channel function, click the [Combination Setting] module function button to open the Combination Setting dialog box for setting. For details, refer to Section 5.3.3 “Combination setting” in the *MX180000A Operation Manual*.

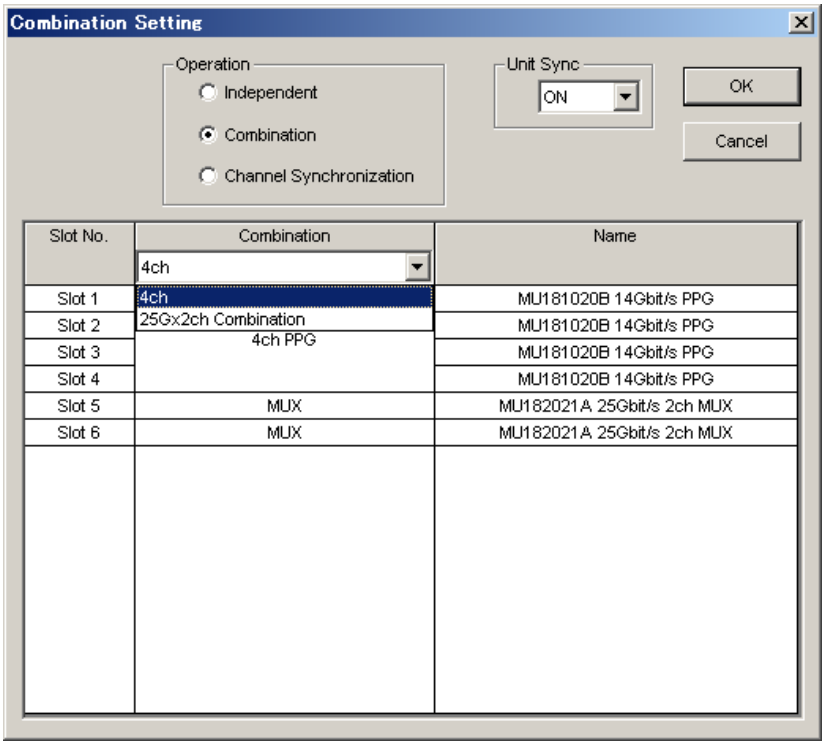


Figure 5.5.2-1 Combination Setting dialog box

Table 5.5.2-1 Screen Layout for Combination Setting

Operation Settings		Contents
Independent		Select when performing MU181020A/B or MU181040A/B independently
Combination	2ch	Select when performing 25 Gbit/s tests
	4ch	Select when performing 40 Gbit/s tests
	25Gx2ch Combination	Select when generating/receiving 25 Gbit/s 2 Ch data
Channel Synchronization	12.5G CH Sync	Select when always outputting with synchronized header bit for PON applications, etc.
	25G CH Sync	Select when always outputting with synchronized header bit between two 25 Gbit/s channels.

Confirm the selected operation by pressing the [OK] button.

5.5.3 Multi Channel Calibration Function

Calibration must be executed to use the Multi Channel function under optimum conditions. This function is required when changing the configuration such as rearranging the modules installed in the main frame (MP1800A or MT1810A).

When calibration is required, a message dialog (Figure 5.5.3-1) is displayed when selecting the Channel Synchronization or Combination setting. To execute Combination, press the [Yes] button.

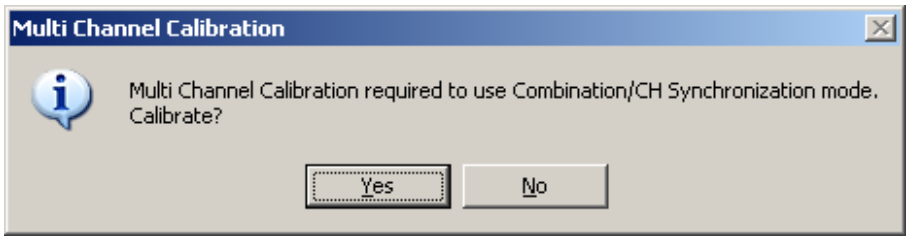


Figure 5.5.3-1 Multi Channel Calibration Requirement Message

Press the [Next] button after confirming the explanation. Calibration requires about 2 to 10 minutes.

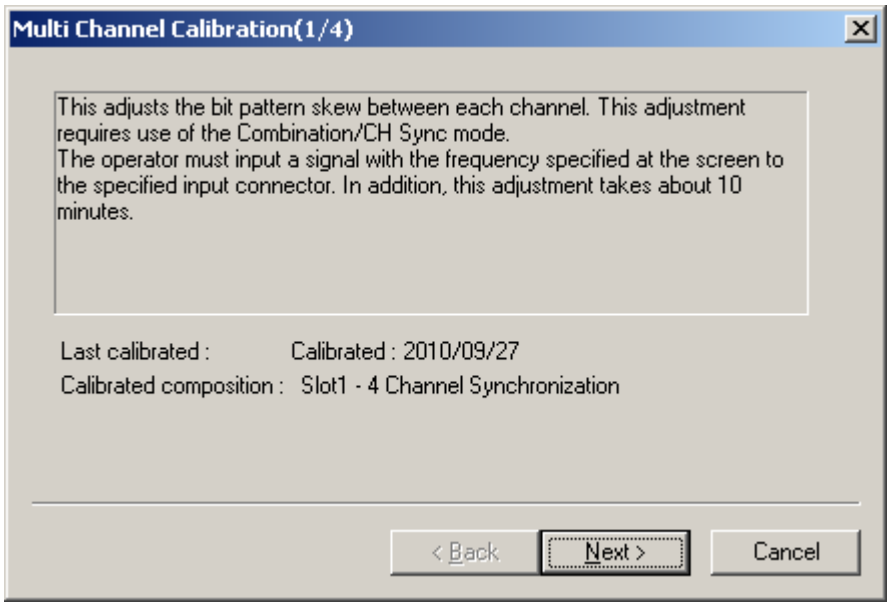


Figure 5.5.3-2 Multi Channel Calibration Screen 1

Press the [Next] button after connecting same-length cables and inputting the clock frequency specified on the screen. When the MU181000A/B is installed in the same main frame with this unit, input the clock from the MU181000A/B to this unit.

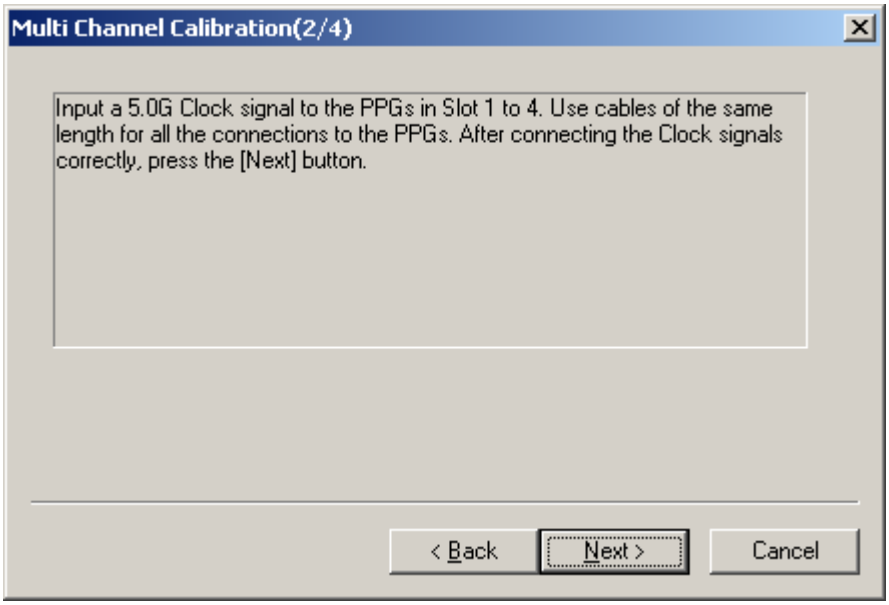


Figure 5.5.3-3 Multi Channel Calibration Screen 2

The calibration progress is displayed by the bar.

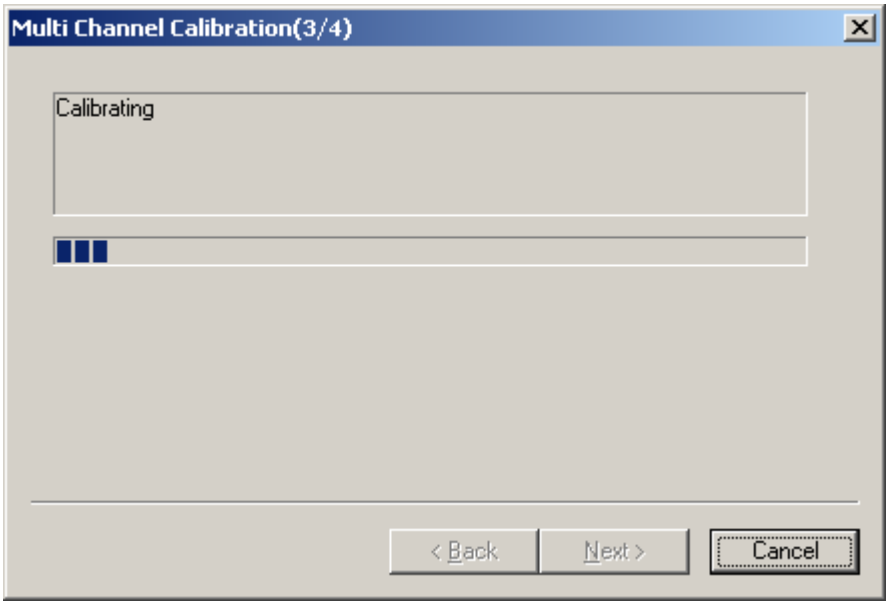


Figure 5.5.3-4 Multi Channel Calibration Screen 3

If the message dialog shown in Figure 5.5.3-5 is displayed during calibration, change the input clock frequency as indicated and press the [Next] button. The calibration clock frequency differs according to whether the unit type is A or B, as shown below:
MU181020A: 5G, 8G, 10G, 12.5G
MU181020B: 5G, 8G, 10G, 12.5G, 14G
Moreover, when both the MU181020A and MU181000A/B synthesizer are installed in the same main frame, it is not necessary to change the frequency.

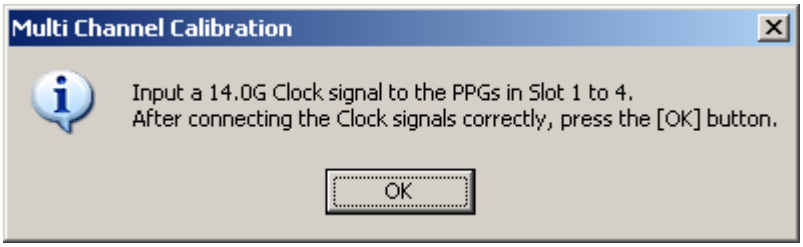


Figure 5.5.3-5 Clock Frequency Change Message

Press the [Finish] button when the screen shown in Figure 5.5.3-6 is displayed to complete the calibration.

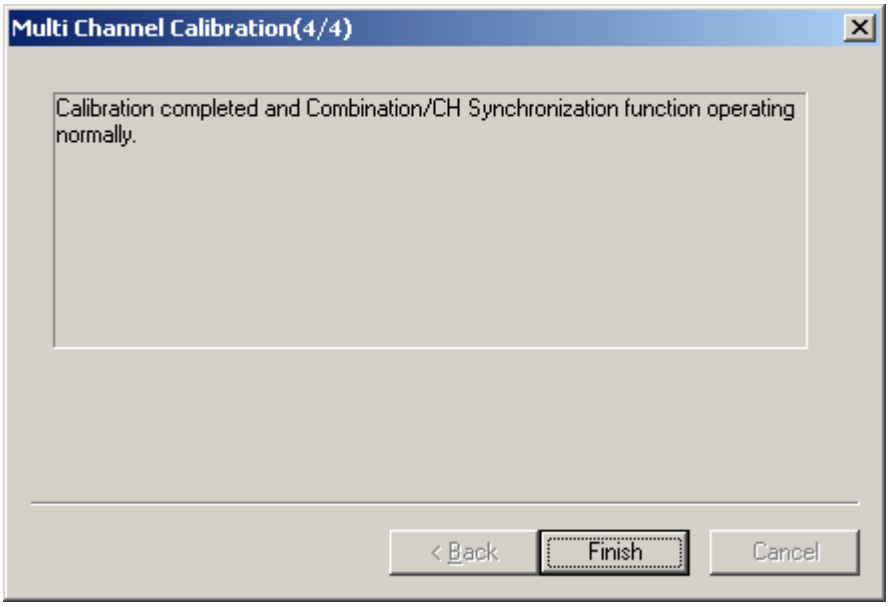


Figure 5.5.3-6 Multi Channel Calibration Screen 4

If the [No] button displayed in the message dialog of Figure 5.5.3-1 is pressed, select [Multi Channel Calibration] from the File menu (Figure 5.5.3-7) to assure the performance.

When the [No] button is pressed, the dialog shown in Figure 5.5.3-8 is displayed; if the check box is selected, this calibration-required dialog will not be displayed again when calibration is required in future.

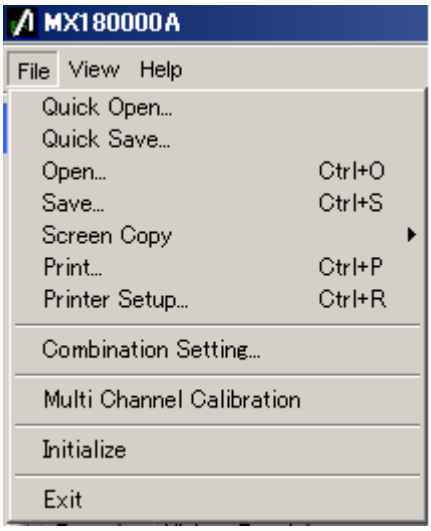


Figure 5.5.3-7 File Menu

Figure 5.5.3-8 Calibration Cancel Confirmation Dialog

After calibration has been completed once, it is not required again if the configuration of units installed in the main frame is not changed.

To confirm whether or not calibration has already been performed, check the Calibration screen (Figure 5.5.3-9).

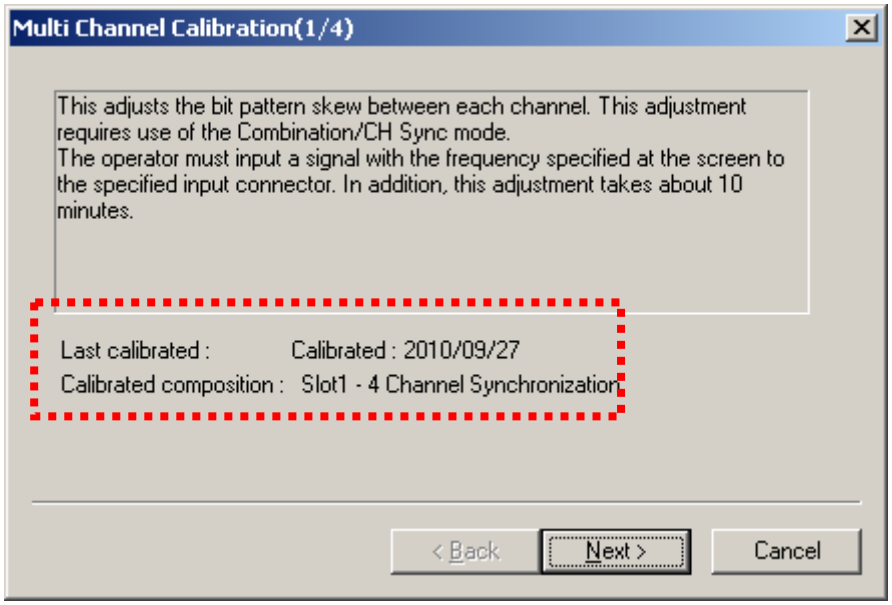


Figure 5.5.3-9 Calibration Execution Verification

Notes:

- If the hardware version is earlier than 1.00.22, the Multi Channel Calibration function cannot be used. Upgrade the version to support the Multi Channel function. Version upgrade requires returning the unit to the factory, so request service from Anritsu or our sales representative.
- It may be necessary to perform calibration several times depending on the Channel Synchronization and Combination selection.

5.6 Unit Sync Function

The Unit Sync function is used to synchronize multiple MP1800A units to generate the same pattern. This section explains how to set the Unit Sync function as well as the operations and restrictions when using this function.

5.6.1 Unit Sync Operation and Restrictions

The Unit Sync function synchronizes multiple main frames by sharing a timing signal between them.

Patterns can be generated and synchronized for up to 16ch by using the Unit Sync function with the Channel Synchronization or Combination functions for synchronizing modules in the main frame.

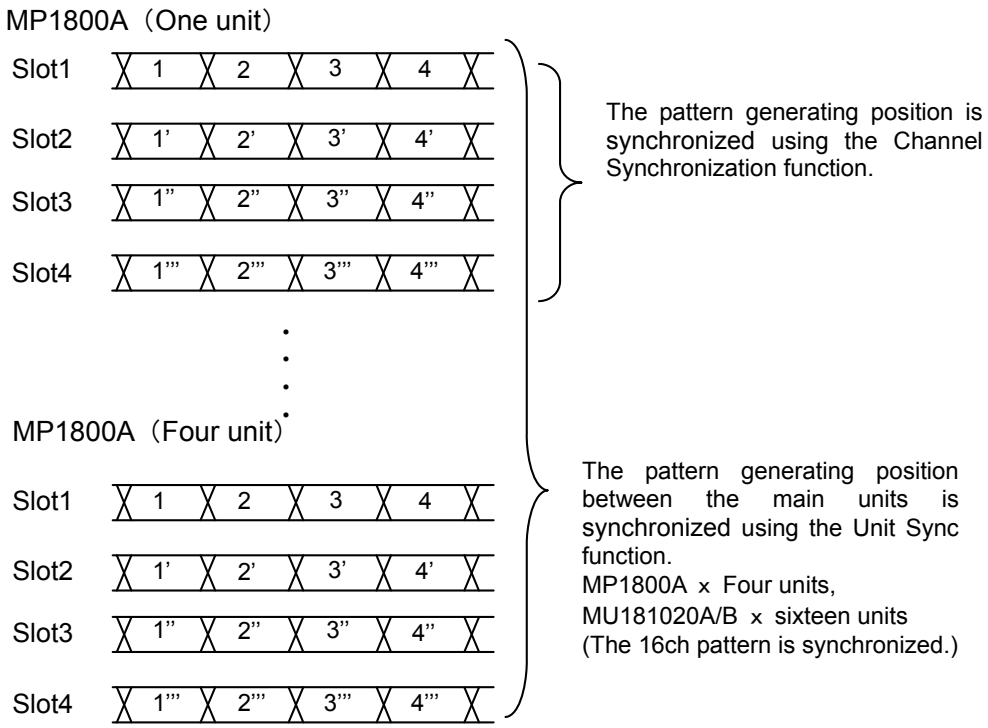


Figure 5.6.1-1 Channel Synchronization Pattern Generation

Since the Unit Sync function has a maximum bit phase error of ±256 bits between main frames, adjustment is required to remove this error. Refer to Appendix E “Preparing to Use Unit Sync Function” for this adjustment procedure.
However, this error does not change unless the operation clock changes. Adjustment is required if the operation clock input is interrupted or changed.

Furthermore, there are following restrictions when using the Unit Sync function:

- Cannot use the Burst function
- Cannot switch Alternate pattern using the external signal
- Cannot switch Mixed Alternate pattern using the external signal
- Cannot control Sequence pattern using the external signal.
- Cannot add error using the external signal
- The Unit Sync function is unavailable when MU181020A/20B and MU181040A/40B are used in the same mainframe.

5.6.2 Unit Sync Setting

To use the Unit Sync function, press [Combination Setting] of the module function buttons and set at the Combination Setting screen.

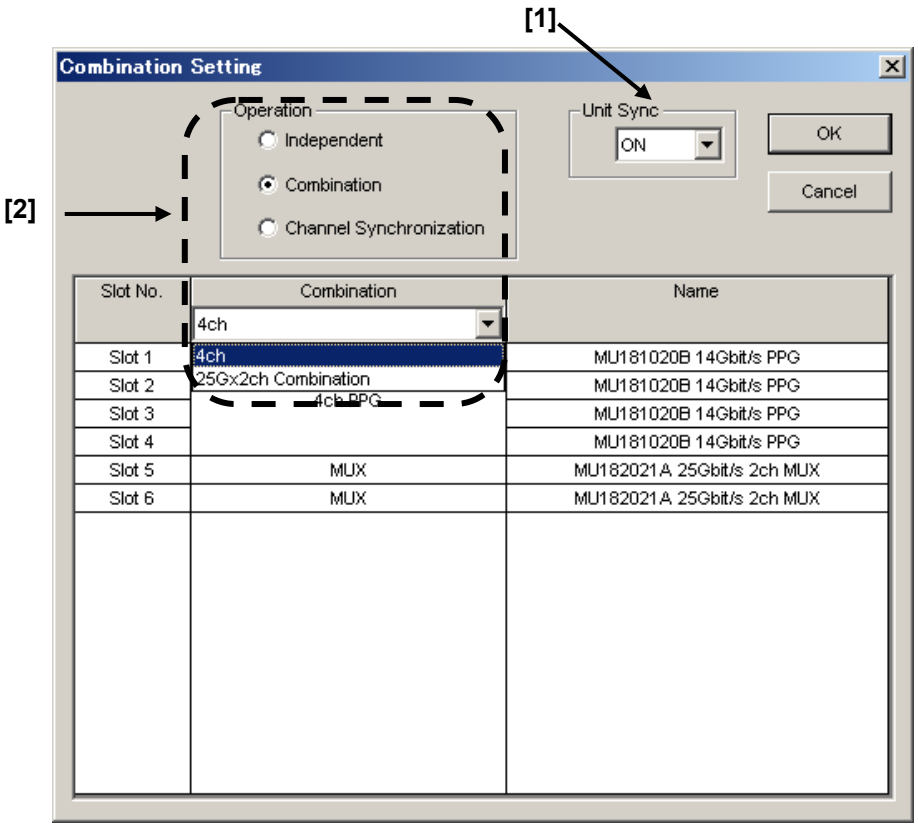


Figure 5.6.2-1 Combination Setting screen

[1] Sets Unit Sync function ON/OFF
Set Unit Sync to ON and press [OK] to enable the function.
Confirmed the message dialog (Figure 5.6.2-2) displayed according to the restrictions in section 5.6.1 when settings are changed.

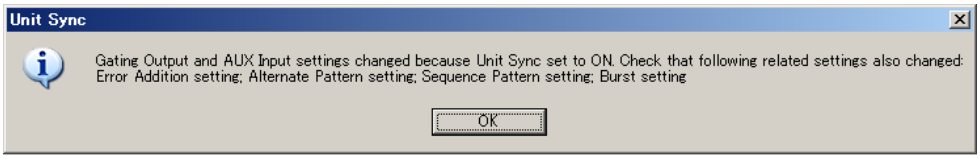


Figure 5.6.2-2 Dialog screen when settings changed at Unit Sync ON

When Unit Sync is ON, the combinations that can be set when Operation is set to either Combination or Channel Synchronization are shown in Table 5.6.2-1.

Table 5.6.2-1 Combination Settings for Unit Sync

Operation	Combination
Combination	4ch
	25G x 2ch Combination
Channel Synchronization	12.5G CH Sync
	25G CH Sync

5.6.3 How to Use Unit Sync Function

This section explains how to use the Unit Sync function. Refer to Appendix E "Preparing to Use Unit Sync Function" in this document for the connections and adjustment procedure when using the Unit Sync function.

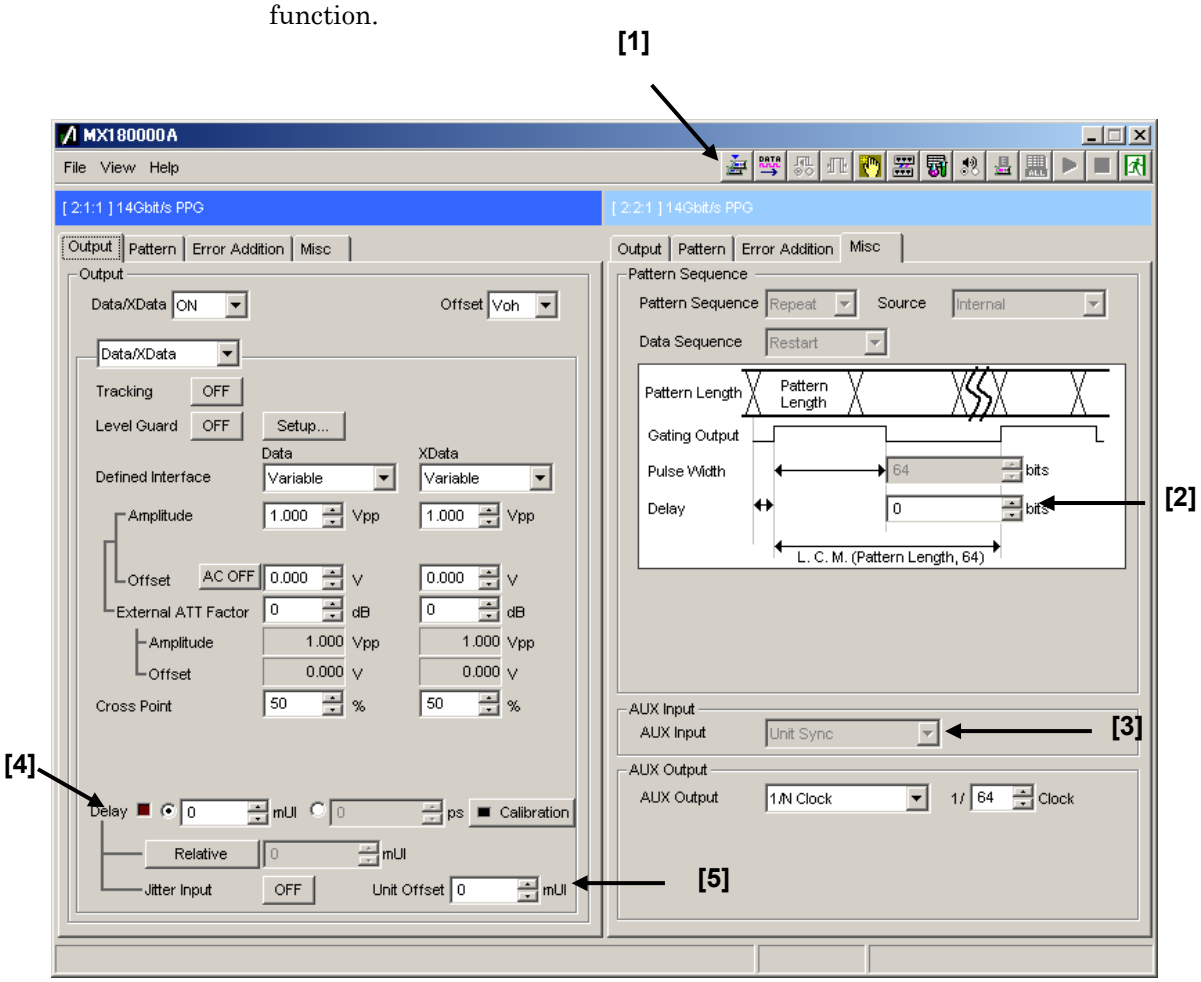


Figure 5.6.3-1 MX180000A Screen

[1] Unit Sync Output

Pressing the button outputs the timing signal for synchronization with the main frame. It is enabled only when Unit Sync is set to ON.

Note:

Resynchronization must be performed again by pressing the button if the operation clock input is interrupted or changed. In addition, it is necessary to adjust the bit skew with the main frame after performing resynchronization.

[2] Gating Output Delay

This sets and adjusts the delay the timing signal for synchronizing with the main frame. The setting resolution is as follows:

Independent/12.5G CH Sync: 64-bit step
25G CH Sync : 128-bit step
25G x 2ch/4ch Combination : 256-bit step

[3] AUX Input

This is a dedicated input for the timing signal for synchronizing with the main frame at Unit Sync ON.

[4] Delay

This adjusts the bit skew of the output pattern between channels by setting the Delay for each MU181020A/B inserted in slots 1 to 4 of the same main frame.

[5] Unit Offset

This sets the offset for the delay at each main frame by adjusting the bit skew of the output pattern between main frames. The setting ranges are as follows, but there are some restrictions depending on the setting of Delay [4].

Independent:
–1000 to +1000 mUI = Delay setting + Unit Offset setting range
Channel Synchronization/Combination:
–64000 to +64000 mUI = Delay setting + Unit Offset setting range.

Chapter 6 Use Example

This chapter provides use examples of measurement using the MU181020A.

6.1 Measuring Optical Transceiver Module (error rate measurement using PRBS pattern)

This section provides an example of how to test the electrical interface input sensitivity of an XFP optical transceiver module by using the MP1800A.

6.1.1 Test method

In the following test example, the MU181020A and MU181040A are mounted onto the MP1800A.
The options configuring the test system are as follows:

MP1800A-014
MU181020A-001, MU181020A-x10
MU181040A-001, MU181040A-x20

1. Connect the GND of the MP1800A and that of the DUT.
2. Connect the power cables.
3. Turn on the MP1800A, and set the measurement conditions as follows.
   (1) Adjust the data output interface of the MU181020A to the input interface of the DUT. In the MU181020A Output tab window, select Data/XData and set Tracking to ON. The Data/XData amplitude and offset setting are applied commonly. This is useful for setting the differential interface data. Set the amplitude and offset according to the input interface of the DUT.
   (2) Configure the settings of the test pattern in the MU181020A or MU181040A Pattern tab window.
   (3) If the XFP module requires a reference clock, make the setting on the MU181020A Misc tab window so that a 1/64 divided clock is output from the AUX Output connector.
   (4) Set the operating bit rate from CMU Bit Rate in the MU181020A Output tab window.
   (5) Adjust the data input interface of the MU181040A to the output interface of the DUT. Select the termination condition from Input Condition in the MU181040A Input tab window. Since the XFP module is connected with the differential interface, select “Differential 100 ohm” and “Tracking”.

(6) Specify the clock for error measurement.
In the Clock field on the MU181040A Input tab window, select "Recovered Clock" from the Selection drop-down list and specify the operating bit rate.

(7) When setting the parameters completely, turn off the MP1800A.

4. Connect the MP1800A and the DUT.

Connect the I/O signals using the supplied coaxial cables (cables equivalent to the supplied ones can also be used). At this time, short the cable cores, using a thin pointed metal stick such as tweezers before connection.

See Figure 6.1.1-1 for connection of the instruments.

Check that the reception data output level of the XFP module falls within the data input range of the MU181040A. If not, adjust the level by using an attenuator.

5. Turn on the MP1800A first, and then DUT.

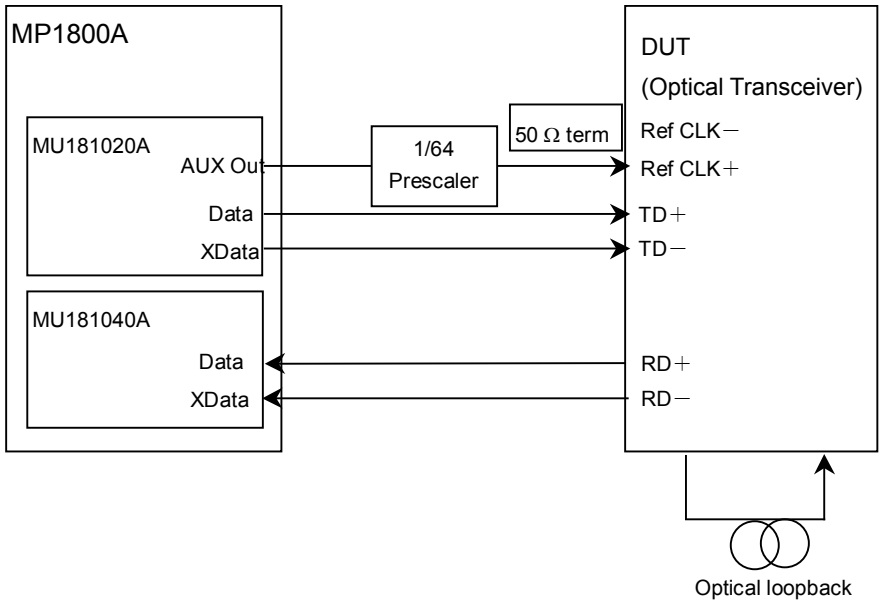


Figure 6.1.1-1 Connection diagram for XFP module evaluation

CAUTION ⚠

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A before changing the cable connection.

6. Enable the signal output of the MU181020A.
   Set Data/XData to ON in the MU181020A Output tab window, and set the Output module function button to “ON”.
7. Adjust the threshold voltage of the MU181040A. When the Auto Adjust function is used, clicking the Auto Adjust module function button on the menu bar automatically adjusts the threshold voltage to the optimum value for the DUT.
8. The BER measurement results are displayed in the MU181040A Result tab window. No error is detected when there is no failure and the connection and settings are correct.
9. Confirm that the DUT operates normally. If so, data input (TD+, TD–) sensitivity measurement can be performed for the DUT by adjusting the output level of the MU181020A.

6.2 Measuring 4:1 MUX (generating 40 Gbit/s PRBS pattern using four MU181020A modules)

This section provides an example of how to test the performance of the 40 GHz band 4:1 MUX IC by using two MP1800A units.

6.2.1 Test method

1. Connect the GND of the MP1800A, device under test (DUT), and demultiplexer (MP1804A 43.5 G DEMUX).
2. Mount four MU181020A modules and one MU181800A 12.5 GHz Clock Distributor (hereinafter, referred to as "MU181800A") onto an MP1800A unit, and mount four MU181040A modules onto the other MP1800A unit.
   The options configuring the test system are as follows:

   MP1800A-x15
   MU181020A-001, MU181020A-x10
   MU181040A-001
3. Connect the power cables.
4. Turn on the MP1800A on which the MU181020A modules are mounted, and set the measurement conditions as follows.
   (1) The mounted four MU181020A modules must be synchronized for testing the MUX IC. Click the Combination module function button and select "4ch combined".
   (2) Adjust the data output interface of the MU181020A to the input interface of the DUT. In the MU181020A Output tab window, adjust Data to the input interface of the DUT, then set the amplitude and offset.
   (3) Set a test pattern.
   A test pattern can be selected from the MU181020A Pattern tab window. When the settings of a channel are changed, the changed settings apply to all the other channels.
   (4) Set the operating bit rate from the MU181020A CMU bit rate window. When "4ch combined" is selected, Channel 1 is forcibly selected for the operating clock.
   (5) When setting the parameters completely, turn off the MP1800A.

5. Turn on the MP1800A on which the MU181040A modules are mounted, and set the measurement conditions as follows.
   (1) Adjust the data input interface of the MU181040A to the output interface of the DUT. Select the interface and termination condition from Input Condition in the MU181040A Input tab window. Since the MP1804A supports 0/–1 V, select "Single-Ended" for Input Condition, "GND" for Termination, and "–0.5 V" for Data threshold.
   (2) In the MU181040A Pattern tab window, select the test pattern that is set in the MU181020A Pattern tab window.
   (3) Specify the clock for error measurement. Select "External Clock" from Clock selection in the MU181040A Input tab window.
   (4) When setting the parameters completely, turn off the MP1800A.
6. Connect the MP1800A, MP1804A, and the DUT.

   Connect the I/O signals, using the supplied coaxial cables (cables equivalent to the supplied ones can also be used). Short the cable cores, using a thin pointed metal stick such as tweezers before connection.

   See Figure 6.2.1-1 for connection of the instruments.

   Check that the MUX output level of the 4:1 MUX IC (DUT) falls within the data input range of the MP1804A. If not, adjust the level by using an attenuator.

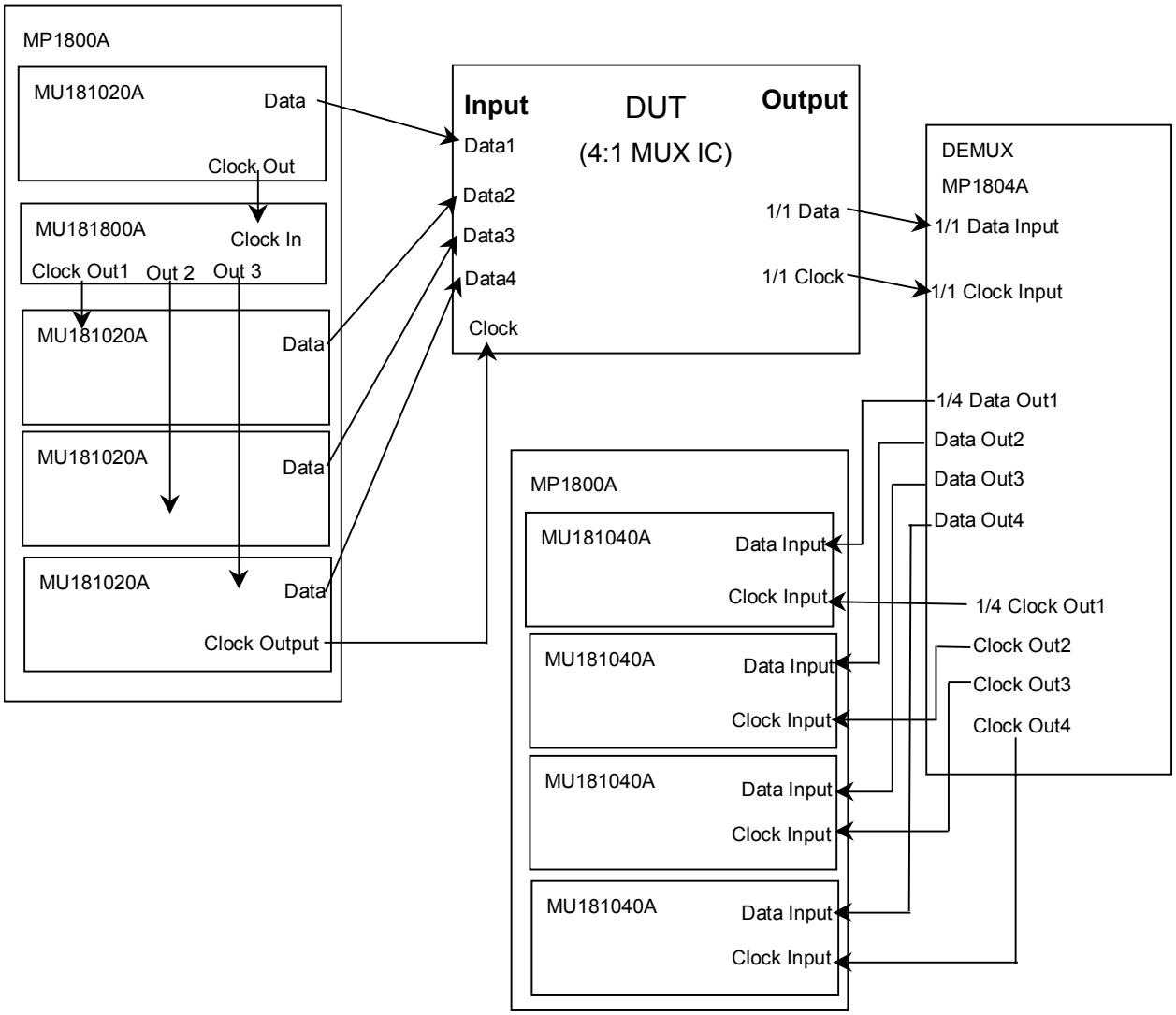


Figure 6.2.1-1 Connection diagram for 4:1 MUX IC evaluation

7. Turn on the measuring instruments in the following order: MP1800A on which MU181040A modules are mounted → MP1804A → DUT → MP1800A on which MU181020A modules are mounted

CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A and MP1804A before changing the cable connection.

8. Enable the signal output of the MU181020A.
   Set Data/XData to ON in the MU181020A Output tab window, and set the Output module function button to "ON".
9. Adjust the threshold voltage and phase of the MP1804A to the optimum values, using the 1/1 Clock and V_{TH} knobs of the MP1804A.
10. Set the threshold voltage and phase of the MU181040A. When the Auto Adjust function is used, clicking the Auto Adjust module function button on the menu bar automatically adjusts the threshold voltage and phase to the optimum values for the DUT.
11. The BER measurement results are displayed in the MU181040A Result tab window. No error is detected when there is no failure and the connection and settings are correct.
12. Confirm that the DUT operates normally. If so, margin measurement can be performed for the 4:1 MUX IC by changing the output level and offset of the MU181020A.

6.3 ONU-OLT Uplink Test (burst signal error rate measurement)

This section provides an example of how to measure the uplink error rate between ONU and OLT in the PON network by using the Burst pattern generation function of the MU181020A.

6.3.1 Test method

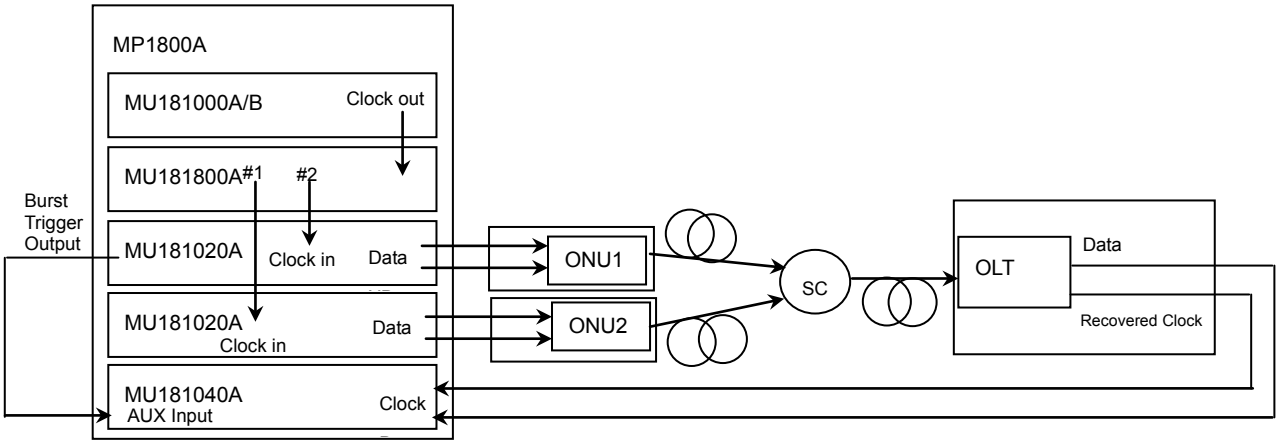
1. Connect the GND of the MP1800A and that of the DUT.
2. Mount two MU181020A modules, one MU181000A, one MU181800A, and one MU181040A onto the MP1800A unit.
   The options configuring the test system are as follows:

   MP1800A-015
   MU181020A-002, MU181020A-x10
   MU181040A-002
3. Connect the power cables.
4. Turn on the MP1800A and set the measurement conditions as follows.
   (1) The two mounted MU181020A modules must be synchronized for the ONU-OLT uplink test. Click the Combination module function button and select “Channel Synchronization”.
   (2) Adjust the data output interface of the MU181020A to the input interface of the DUT. In the MU181020A Output tab window, adjust Data to the input interface of the DUT, then set the amplitude and offset.
   (3) Set the Burst pattern generation timing and the test pattern. To set the Burst pattern generation timing, select “Burst” from the Pattern Sequence drop-down list in the Misc tab window, and then specify the timing.
   (4) Specify the generation pattern from the Test Pattern drop-down list in the Pattern tab window. The timing and pattern type can be set independently for each channel.
   (5) Set the operating frequency in the Synthesizer window.
   (6) Adjust the data input interface of the MU181040A to the output interface of the DUT. Specify the termination condition from the MU181040A Input tab window. For the test pattern, write data of two channels generated from the MU181020A and specify the measurement area by Mask setting from the Pattern tab window, to generate an error detection pattern. Set Burst for the AUX Input setting on the Misc tab window.
   (7) Turn off the MP1800A when setting the parameters completely.

5. Connect the MP1800A and the DUT.

   Connect the I/O signals, using the supplied coaxial cables (cables equivalent to the supplied ones can also be used). At this time, short the cable cores, using a thin pointed metal stick such as tweezers before connection.

   See Figure 6.3.1-1 for connection of the instruments.



Note:

MU181800A is not required when using MU181000B.

Figure 6.3.1-1 Connection diagram for ONU-OLT uplink test

6. Turn on the DUT first, and then the MP1800A.

⚠ CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1800A before changing the cable connection.

7. Enable the signal output of the MU181020A.
   Set Data/XData to ON in the MU181020A Output tab window, and set the Output module function button to "ON".
8. Set the threshold voltage and phase of the MU181040A. When the Auto Adjust function is used, clicking the Auto Adjust module function button on the menu bar automatically adjusts the threshold voltage and phase to the optimum value for the DUT.
9. The BER measurement results are displayed in the MU181040A Result tab window. No error is detected when there is no failure and the connection and settings are correct.

10. Confirm that the DUT operates normally. If so, load measurement can be performed for the DUT, by changing the interval between the ONU channels with the Phase Adjust function provided in the MU181020A Output tab window, and by changing the Burst signal interval from Delay on the Misc tab window.

Chapter 7 Performance Test

This chapter describes the performance testing of the MU181020A.

7.1 Overview

Performance tests are executed to check that the major functions of the MU181020A meet the required specifications. Execute performance tests at acceptance inspection, operation check after repair, and periodic (once every six months) testing.

7.2 Devices Required for Performance Tests

Before starting performance tests, warm up the MX181020A and the measuring instruments for at least 30 minutes. Table 7.2-1 shows the devices required for performance tests.

Table 7.2-1 Devices required for performance test

Device Name	Required Performance
Error detector (MP1800A+MU181040A)	Operating frequency: 100 MHz to 12.5 GHz Data input sensitivity: 100 mVp-p or more
Error detector (MP1800A+MU181040B)	Operating frequency: 100 MHz to 14 GHz Data input sensitivity: 100 mVp-p or more
Sampling Oscilloscope	Electrical interface: 50 GHz or more band
Signal generator (MP1800A+MU181000A/B, MG3690 series)	At MU181020A evaluation Operating frequency: 100 MHz to 12.5 GHz Output level: 400 to 2000 mVp-p Waveform: 100 to 500 MHz rectangular wave > 500 MHz rectangular wave or sine wave When evaluating the MU181020B, use the MG3690 series in addition to the above. Operating frequency: 12.5 GHz to 14 GHz Output level: 400 to 1500 mVp-p Waveform: Rectangular wave or sine wave

Note:

Before starting the performance tests, warm up the device under test and the measuring instruments for at least 30 minutes and wait until they become sufficiently stabilized, unless otherwise specified. Additional conditions are required for maximum measurement accuracy: measurements must be performed at room temperature, fluctuations of AC power supply voltage must be small, and noise, vibration, dust, and humidity must be insignificant.

7.3 Performance Test Items

This section describes the following test items.

(1) Operating frequency range

(2) Waveform

7.3.1 Operating frequency range

(1) Specifications

Table 7.3.1-1 Specifications

Option	Specifications
MU181020A-001	9.8 to 12.5 GHz
MU181020A-002	0.1 to 12.5 GHz
MU181020B-002	0.1 to 14 GHz
MU181020B-003	0.1 to 14.05 GHz
MU181020B-005	0.1 to 14.1 GHz

(2) Device connection

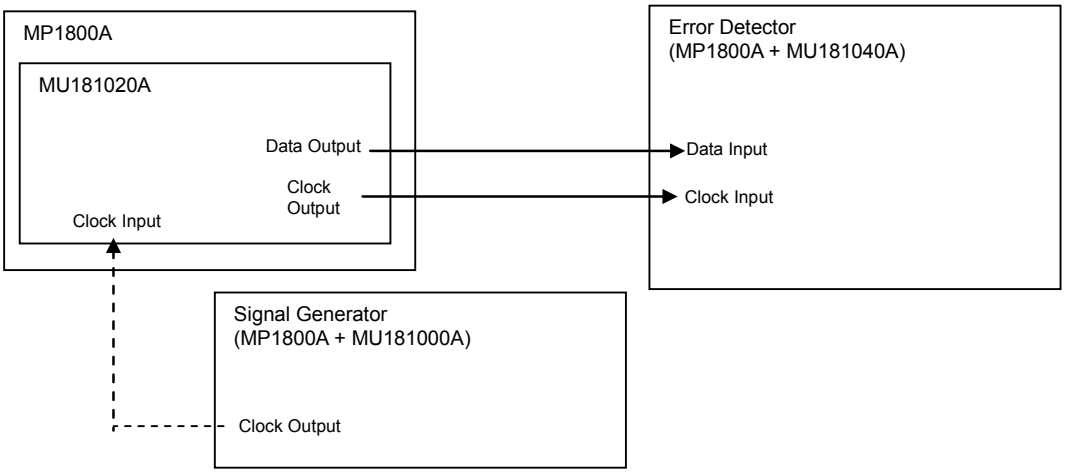


Figure 7.3.1-1 Connection diagram for operating frequency range test

(3) Test procedure

1. Mount the MU181020A onto the MP1800A, and turn on the MP1800A with the cables unconnected.
2. When the MU181020A-001 is installed, set Reference Clock to Internal and set Frequency to 12.5 GHz on the MU181020A Output CMU Bit Rate window.
   When the MU181020A-002 is installed, the clock is supplied from the external signal source. Set the output level in advance so that an excessive voltage is applied.

3. Set the Data signal output amplitude of the MU181020A to 500 mVp-p, offset (Vth) to 0 V, test pattern to PRBS 31, and mark ratio to 1/2.
4. Set the Clock signal output amplitude of the MU181020A to 500 mVp-p and offset (Vth) to 0 V.
5. After setting the parameters, turn off the MP1800A.
6. Connect cables among measuring instruments by referring to Figure 7.3.1-1.
7. Turn on the MP1800A and the measuring instruments, and warm them up.
8. After warming up the instruments, enable the MP1800A signal output (ON) and output signals.
9. Adjust the phase and threshold voltage of the MU181040A to the optimum values.
10. Check that no error is detected by the MU181040A.
11. Change the operating frequency and check if no error occurs within the rated operating frequency range.

7.3.2 Waveform evaluation test

(1) Specifications

Table 7.3.2-1 Specifications for MU181020A

Option	Specifications
MU181020A-001 9.8 to 12.5 Gbit/s	Levels: High: –0.2 to 0.1 V, Low: –0.65 to –0.4 V Cross Point: 50% ±15% Tr/Tf: Typ.30 ps (20 to 80%) (≥5 Gbit/s) Typ.40 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 15 psp-p*
MU181020A-002 0.1 to 12.5 Gbit/s	Levels: High: –0.25 to 0.05 V, Low: –1.4 to –0.85 V Cross Point: 50% ±15% Tr/Tf: Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ. 45 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 10 psp-p*
MU181020A-x10 Variable Data Output (0.05 to 0.8 Vp-p) Retrofit	Level: 0.05 to 0.80 Vp-p Offset: –2.0 to +3.3 Voh Cross Point: 30 to 70%, 1% steps (Not independent) Tr/Tf: Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 15 ps p-p (when installed in MU181020A-001)* Typ. 10 ps p-p (when installed in MU181020A-002)* Waveform distortion: Typ. ±14% 10 Gbit/s (amplitude: 0.5 to 0.8 V)
MU181020A-x11 Variable Data Output (0.25 to 2.5 Vp-p) Retrofit	Level: 0.25 to 2.50 Vp-p Offset: –2.0 to C3.3 Voh Cross Point: 30 to 70%, 1% steps (Independent) Tr/Tf: Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 15 ps p-p (when installed in MU181020A-001) Typ. 10 ps p-p (when installed in MU181020A-002) Waveform distortion: Typ. 25 mV ±6% 10 Gbit/s

*: The jitter specification value is defined assuming that an oscilloscope with residential jitter less than 200 fs (RMS) is used.

Table 7.3.2-1 Specifications for MU181020A (continued)

Option	Specifications
MU181020A-x12 High Performance Data Output (0.05 to 2.0 Vp-p) Retrofit	Level: 0.05 to 2.0 Vp-p Offset: –2.0 to + 3.3 Voh Cross Point: 20 to 80%, 1% step (Independent) Tr/Tf : Typ. 20 ps, (20 to 80%) (at 10 G, 12.5 Gbit/s, 2.0 Vp-p) Typ. 25 ps, (10 to 90%) (at 10 G, 12.5 Gbit/s, 2.0 Vp-p) Total Jitter: Typ. 15 psp-p (when installed in MU181020A-001)* Typ. 8 psp-p (when installed in MU181020A-002)* Waveform distortion: Typ.25 mV ±6% (10 Gbit/s)
MU181020A-x13 Data Output (0.5 to 3.5 Vp-p) Retrofit	Level: 0.5 to 3.5 Vp-p Offset: –2.0 to +3.3 Voh Cross Point: 20.0 to 90.0%, 0.1% Step (Independent) Tr/Tf: Typ. 25 ps (20 to 80%) (at 10 G, 12.5 Gbit/s, 3.5 Vp-p) Total Jitter: Typ.8 psp-p (when installed in MU181020A-001/002, at 10 Gbit/s)* Waveform distortion: Typ.25 mV±10% (10 Gbit/s)

Table 7.3.2-2 Specifications for MU181020B

Option	Specifications
MU181020B-002 0.1 to 14 Gbit/s or MU181020B-003 0.1 to 14.05 Gbit/s or MU181020B-005 0.1 to 14.1 Gbit/s	Levels: High: –0.25 to 0.05 V, Low: –1.4 to –0.85 V Cross Point: 50% ±15% Tr/Tf: Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ. 45 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 10 psp-p*
MU181020B-x11 Variable Data Output (0.25 to 2.5 Vp-p) Retrofit	Level: 0.25 to 2.50 Vp-p Offset: –2.0 to C3.3 Voh Cross Point: 30 to 70%, 1% steps (Independent) Tr/Tf: Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s) Total Jitter: Typ. 10 ps p-p (when installed in MU181020B-002) Waveform distortion: Typ. 25 mV ±6% 10 Gbit/s
MU181020B-x12 High Performance Data Output (0.05 to 2.0 Vp-p) Retrofit	Level: 0.05 to 2.0 Vp-p Offset: –2.0 to + 3.3 Voh Cross Point: 20 to 80%, 1% step (Independent) Tr/Tf : Typ. 20 ps, (20 to 80%) (at 10 G, 12.5, 14 Gbit/s, 2.0 Vp-p) Typ. 25 ps, (10 to 90%) (at 10 G, 12.5, 14 Gbit/s, 2.0 Vp-p) Total Jitter: Typ. 8 psp-p (when installed in MU181020B-002)* Waveform distortion: Typ.25 mV ±6% (10 Gbit/s)
MU181020B-x13 Data Output (0.5 to 3.5 Vp-p) Retrofit	Level: 0.5 to 3.5 Vp-p Offset: –2.0 to +3.3 Voh Cross Point: 20.0 to 90.0%, 0.1% Step (Independent) Tr/Tf : Typ. 25 ps (20 to 80%) (at 10 G, 12.5 Gbit/s, 3.5 Vp-p) Total Jitter: Typ.8 psp-p (when installed in MU181020B-002, at 10 Gbit/s)* Waveform distortion: Typ.25 mV±10% (10 Gbit/s)

*: The jitter specification value is defined assuming that an oscilloscope with residential jitter less than 200 fs (RMS) is used.

(2) Device connection

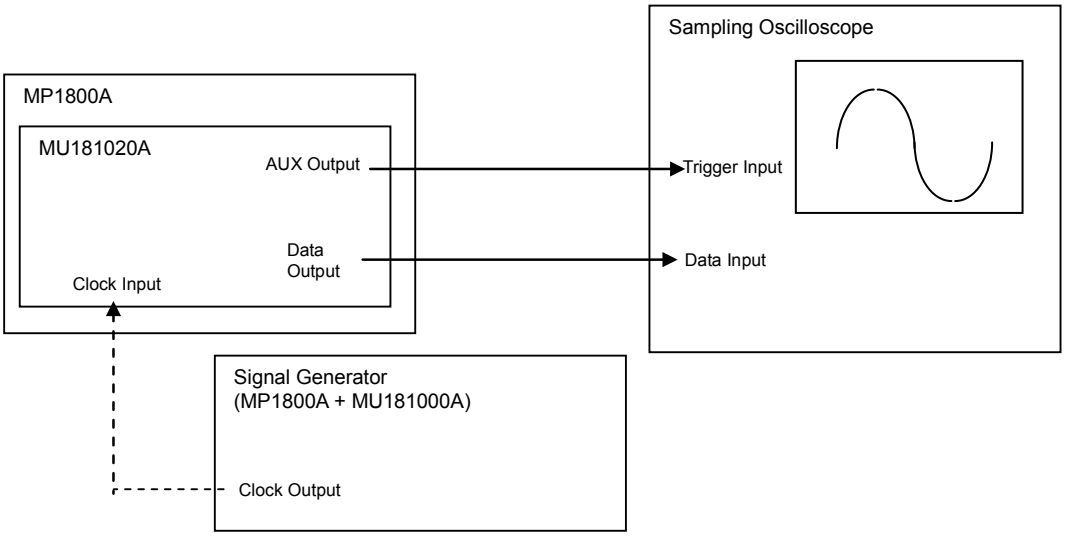


Figure 7.3.2-1 Connection diagram for waveform test

(3) Test procedure

1. Mount the MU181020A onto the MP1800A, and turn on the MP1800A with the cables unconnected.
2. Set the Data output amplitude, offset, and cross point to be tested in the MU181020A Output tab window.
3. Set the test pattern in the MU181020A Pattern tab window. Since the specification parameters are evaluated by observing an Eye pattern, set the test pattern to PRBS 31, and the mark ratio to 1/2.
4. Configure the trigger signal setting. Select 1/N Clock in the AUX Output area on the MU181020A Misc tab window, and set the division ratio according to the sampling oscilloscope used.
5. When the MU181020A-001 is installed, configure the settings of the clock used in the MU181020A Output CMU Bit Rate window.
   When the MU181020A-002 is installed, the clock is supplied from the external signal source. Set the output level in advance so that an excessive voltage is applied.
6. Turn off the MP1800A after setting the parameters.
7. Connect the cables among the measuring instruments, referring to Figure 7.3.2-1.
8. Turn on the MP1800A and the measuring instruments, and warm them up.

9. After warming up the instruments, enable the MP1800A signal output (ON) and output signals.
10. Observe the output waveform on the sampling oscilloscope, and check that all the items conform to the specifications.

Chapter 8 Maintenance

This chapter describes the maintenance of the MU181020A.

8.1 Daily Maintenance

- Wipe off any external stains with a cloth damped with diluted mild detergent.
- Vacuum away any accumulated dust or dirt with a vacuum cleaner.
- Tighten any loose parts fixed with screws, using the specified tools.

8.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MU181020A prior to storage.
Avoid storing the MU181020A in any of the following locations:

- Where there is direct sunlight
- Where there is dust
- Where humidity is high and dew may accumulate
- Where chemically active gases are present
- Where the MU181020A may become oxidized
- Where strong vibrations are present
- Under either of the following temperature and humidity conditions:
  Temperature range of ≤–20°C or ≥60°C
  Humidity range of ≥85%

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to 30°C
- Humidity range of 40 to 75%
- Slight daily fluctuation in temperature and humidity

8.3 Transportation

Use the original packing materials, if possible, when packing the MU181020A for transport. If you do not have the original packing materials, pack the MU181020A according to the following procedure. When handling the MU181020A, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

1. Use a dry cloth to wipe off any stain or dust on the exterior of the MU181020A.
2. Check for loose or missing screws.
3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MU181020A with a sheet of polyethylene. Finally, cover with moisture-proof paper.
4. Place the wrapped MU181020A into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
5. During transportation, place it under an environment that meets the conditions described in Section 8.2 “Cautions on Storage”.

8.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer Series for long-term stable performance. Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item.

8.5 Disposal

Confirm the notes described in the Signal Quality Analyzer Series Installation Guide and observe national and local regulations when disposing of the MU181020A.

Chapter 9 Troubleshooting

This chapter describes how to check whether a failure has arisen when an error occurs during the operation of the MU181020A.

9.1 Problems Discovered during Module Replacement

Table 9.1-1 Remedies for problems discovered during replacement of module

Symptom	Location to Check	Remedy
A module is not recognized.	Is the module installed properly?	Install the module again by referring to Section 2.3 "Installing and Removing Modules" in the installation guide.
	Are the appropriate modules installed?	To check the appropriate modules and software version of the MU181020A/B, access to "MP1800 Series Signal Quality" on your Web site (http://www.anritsu.com). Right-click the "MP1800 Series Signal Quality" and you can access to your area website. If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

9.2 Problems Discovered during Output Waveform Observation

Table 9.2-1 Remedies for problems discovered during waveform observation

Symptom	Location to Check	Remedy
Output waveform cannot be monitored normally.	Is the [Data/XData] or [Clock/XClock] on the Output tab window set to ON?	In the Output tab window, set [Data/XData] or [Clock/XClock] to be output to ON. When the module function button [Output ON/OFF] is enabled, click it to set to ON.
	Is module function button [Output ON/OFF] is set to ON?	Click the module function button [Output ON/OFF] to ON.
	Is the operating clock supplied normally?	When using the internal clock, check the bit rate setting. When the clock is supplied externally, check the connection interface. Refer to Section 3.1 "Panel Layout" for the interface.
	Is the trigger clock set correctly?	It is recommended to use the signal output from AUX output connector as the trigger clock. Check the AUX output connector settings and interface with the sampling oscilloscope to be measured.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.

9.3 Problems Discovered during Error Rate Measurement

Table 9.3-1 Remedies for problems discovered during error rate measurement

Symptom	Location to Check	Remedy
An error occurs.	Is the connection interface with the DUT to be measured correct?	Check that the data rate, level, offset and termination conditions are the same.
	Are the logical patterns correctly set on the MU181020A and the MU181040A error detector (ED)?	Check if the patterns generated by the MU181020A are set such that they can be received by the DUT, and if the set patterns generated by the DUT and detected by the ED are the same. If the DUT outputs the patterns from the MU181020A as they are, connect the MU181020A and ED directly to check if an error is detected.
	Is the error addition function set to off?	Check that the [Error Addition] switch on the Error Addition screen is set to off.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use cables or connectors with good high-frequency characteristics.
	Are sufficient phase margin and bias margin are secured?	Adjust the phase and offset to be optimal between the MU181020A and the DUT as well as between the DUT and ED, respectively.

If a problem cannot be solved using any of the items listed above, perform initialization and check the items again. If the problem still occurs, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the CD version.

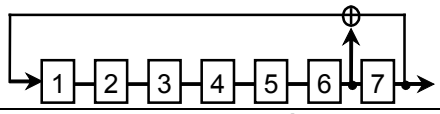
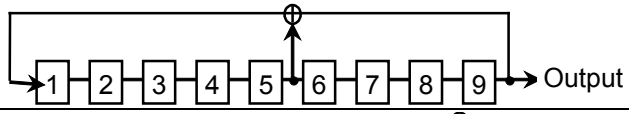
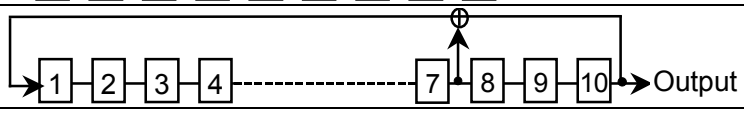
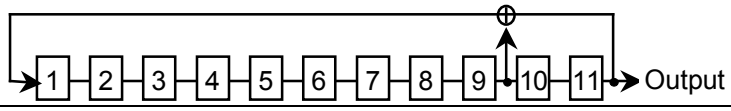
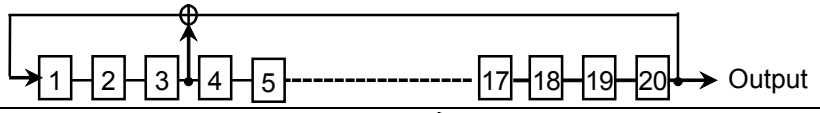
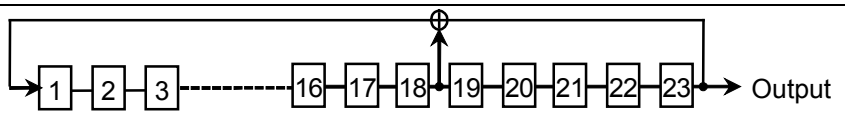
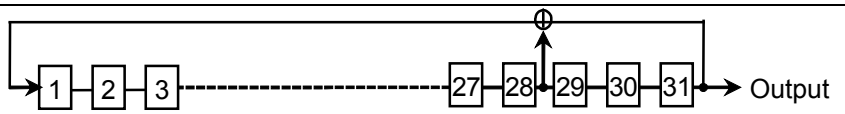
A.1 Pseudo-Random Pattern

Table A.1-1 shows the principle of pseudo-random pattern generation. A pseudo-random pattern is expressed in an N-th degree generating polynomial, with one cycle of $2^n - 1$. For a PRBS pattern with a cycle of $2^n - 1$, a pattern of successive "1s" for the number N is generated once in a cycle.

For the output level of the PRBS pattern, "1" indicates the low level and "0" indicates the high level when Logic is set to POS (positive).

The mark ratios of the PRBS pattern are generated as shown in the block diagrams of Table A.1-1. There are four types of mark ratios: 1/2, 1/4, 1/8, and 0/8 (all 0). In the case of 1/2 and 1/4, the amount of the bit shift can be selected from 1 bit or 3 bits, according to the generation method.

Table A.1-1 Principle of pseudo-random pattern generation

Cycle	Generating polynomial	Pattern generation block diagram
$2^7 - 1$	$1 + X^6 + X^7$	
$2^9 - 1$	$1 + X^5 + X^9$	
$2^{10} - 1$	$1 + X^7 + X^{10}$	
$2^{11} - 1$	$1 + X^9 + X^{11}$	
$2^{15} - 1$	$1 + X^{14} + X^{15}$	
$2^{20} - 1$	$1 + X^3 + X^{20}$	
$2^{23} - 1$	$1 + X^{18} + X^{23}$	
$2^{31} - 1$	$1 + X^{28} + X^{31}$	

N: Shift register (N=1, 2, 3….)

⊕: Exclusive OR

B.1 List of Initialized Settings

This appendix shows the MU181020A settings that are initialized to the defaults at factory shipment.

In addition, All settings can be initialized using the Initialize pull-down from the File menu.

Table B.1-1 List of Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Data/XData Offset ON/OFF			ON
	Clock/XClock Offset ON/OFF (MU181020A-x21, MU181020B-x21)			ON
	Amplitude Offset			Voh
	Data/XData	Tracking		OFF
		Level Guard		OFF
		Level Guard Setup	Amplitude	0.800 Vp-p (MU181020A-x10) 2.500 Vp-p (MU181020A-x11, MU181020B-x11) 2.000 Vp-p (MU181020A-x12, MU181020B-x12) 3.500 Vp-p (MU181020A-x13, MU181020B-x13)
			Offset limit	–2.800 to 3.300 V (MU181020A-x10) –4.500 to 3.300 V (MU181020A-x11, MU181020B-x11) –4.000 to 3.300 V (MU181020A-x12, MU181020B-x12) –4.000 to 3.300 V (MU181020A-x13, MU181020B-x13)
		Defined Interface		Variable
			Amplitude	1.000 Vp-p 0.800 Vp-p (MU181020A-x10)
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
		Cross Point		50%
		Delay		0 mUI
			Calibration	–

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Clock/XClock (MU181020A-x21, MU181020B-x21)	Tracking		OFF
		Level Guard		OFF
		Level Guard Setup	Amplitude	2.000 Vp–p
			Offset limit	–4.000 to 3.300 V
		Defined Interface		Variable
			Amplitude	1.000 Vp–p
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
		Duty		0
	CMU Bit-Rate (MU181020A–x01)	Reference Clock		Internal
		External Clock		1/1
		Operation Rate		1/1
		Frequency	Frequency	12500
			Frequency Resolution	MHz
Pattern	PRBS	Number of Rows		15
		Logic		POS
		Mark Ratio		1/2
	Zero-Substitution	Number of Rows		15
		Zero-substitution Length		1 bit
		Additional Bit		1
	Data	Data Pattern		2 bit In the case of 2 Ch Combination: 4 bits In the case of 4 Ch Combination: 8 bits
	Alternate	Loop Control		Internal
		Alternate Pattern		128 bits
		Loop Time		1

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern (continued)	Mixed Data	Logic		POS
		Block count		1
		Row Length		768 bits In the case of 2 Ch Combination: 1,536 bits In the case of 4 Ch Combination: 3,072 bits
		Data Length		512 bits In the case of 2 Ch Combination: 1,024 bits In the case of 4 Ch Combination: 2,048 bits
		Row count		1
		PRBS	Pattern	PRBS15
			Mark Ratio	1/2
		Scramble		OFF
		Scramble Setup		All OFF
		PRBS Sequence		Consecutive
	Mixed Alternate	Logic		POS
		Loop Control		Internal
		Loop Time		1
		Block count		1
		Row Length		768 bits
		Data Length		512 bits
		Row count		1
		PRBS	Pattern	PRBS15
			Mark Ratio	1/2
		Scramble		OFF
		Scramble Setup		All OFF
		PRBS Sequence		Consecutive
	Sequence	Logic		POS
		Pair ED		None
		Condition		–
		Manual		–
		Transmit		–
		Data Length		MU181020A: 8,192 bit MU181020B: 16,384 bit

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern (continued)	Pattern Editor	Zoom		x 1
		Block count		1
		Row Length		768 bits In the case of 2 Ch Combination: 1,536 bits In the case of 4 Ch Combination: 3,072 bits
		Data Length	Data	2 bits In the case of 2 Ch Combination: 4 bits In the case of 4 Ch Combination: 8 bits
			Alternate	128 bits
			Mixed	512 bits In the case of 2 Ch Combination: 1,024 bits (Mixed-Data) In the case of 4 Ch Combination: 2,048 bits (Mixed-Data)
			Sequence	8192 bits
		Row count		1
		Alternate		A
Error Addition	Error Addition			OFF
		Source		Internal
		Variation		Repeat
		Route		Select, 1
		Error Rate		1E–3
		When test pattern is Alternate: Area A/B		A&B
		When test pattern is Mixed: Row 1		Data: Unselected PRBS: Unselected
		When test pattern is Sequence: Block		Unselected

Table B.1-1 List of Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Misc	Pattern Sequence			Repeat
		Repeat	Pulse Width	64 bits
			Delay	0
		Burst	Source	Internal
			Data Sequence	Restart
			Enable Period	128 000 bits 2 Ch Combination: Default × 2 4 Ch Combination: Default × 4
			Burst Cycle	12 800 000 bits 2 Ch Combination: Default × 2 4 Ch Combination: Default × 4
			Delay	0 bits
			Pulse Width	128 000 bits 2 Ch Combination: Default × 2 4 Ch Combination: Default × 4
	Aux Input			Error Injection
	Aux Output			1/N Clock
		1/N Clock		1/64 clock
		Pattern Sync	PRBS, Zero Substitution, Data: Position	 1 bits
			Alternate: Position	A 1 bits
			Mixed Data: Block No. Row No.	 1 1
			Mixed Alternate: Alternate Content Block No. Row No.	 A 1 1
			Sequence: Block No. Position	 1 1 bits
		Burst Output 2	Delay	0
			Pulse Width	128 000 bits 2 Ch Combination: Default × 2 4 Ch Combination: Default × 4

Note:

When the Initialize function is executed in Combination or Channel Synchronization status, Independent, which is the initial status, is restored.

Appendix C Setting Restrictions

C.1 Setting Restrictions

This appendix describes restrictions due to options or set parameters, and the conditions for using the Combination and Channel Synchronization functions.

C.1.1 Setting range of offset and amplitude

■ Relationship between offset reference value and amplitude

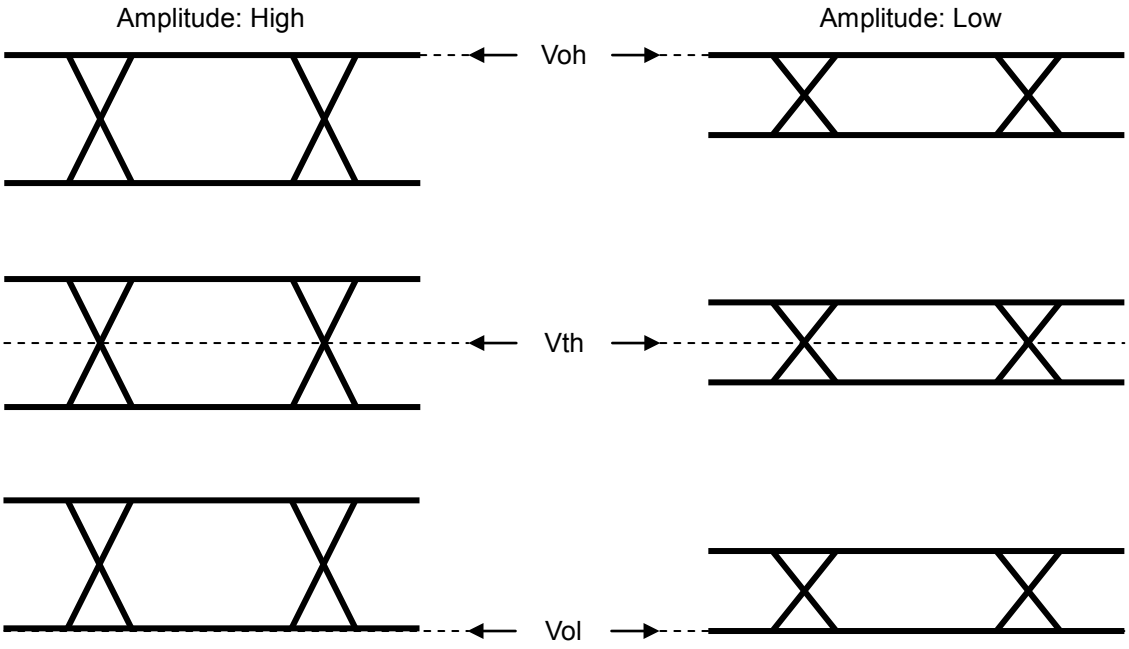


Figure C.1.1-1 Relationship between offset reference value and amplitude

C.1.1.1 MU181020A-x10 Variable Data Output (0.05 to 0.8 Vp-p)

<Specification>
Amplitude: 0.05 to 0.8 Vp-p
Offset: –2.0 to +3.3 V (Voh)

(a) Voh

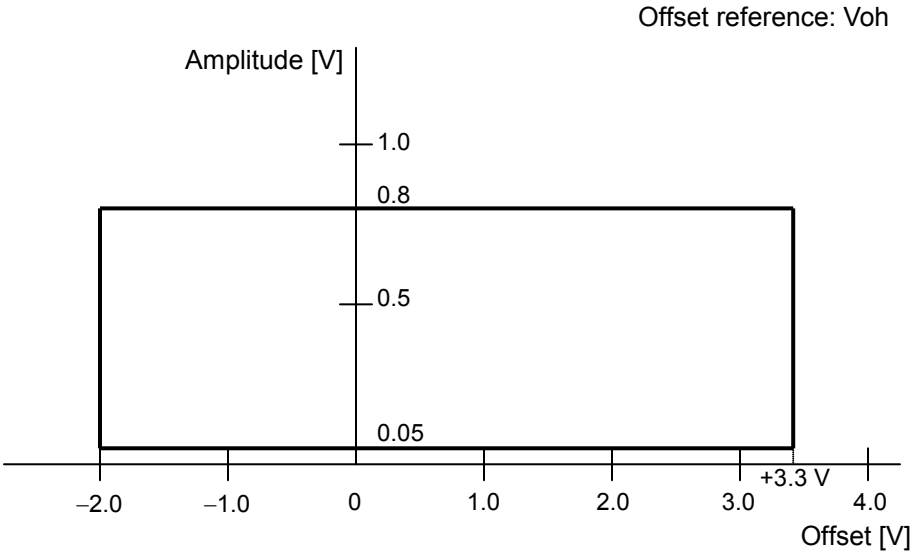


Figure C.1.1.1-1 Setting range of amplitude and offset based on offset reference (Voh) (MU181020A-x10)

(b) Vth

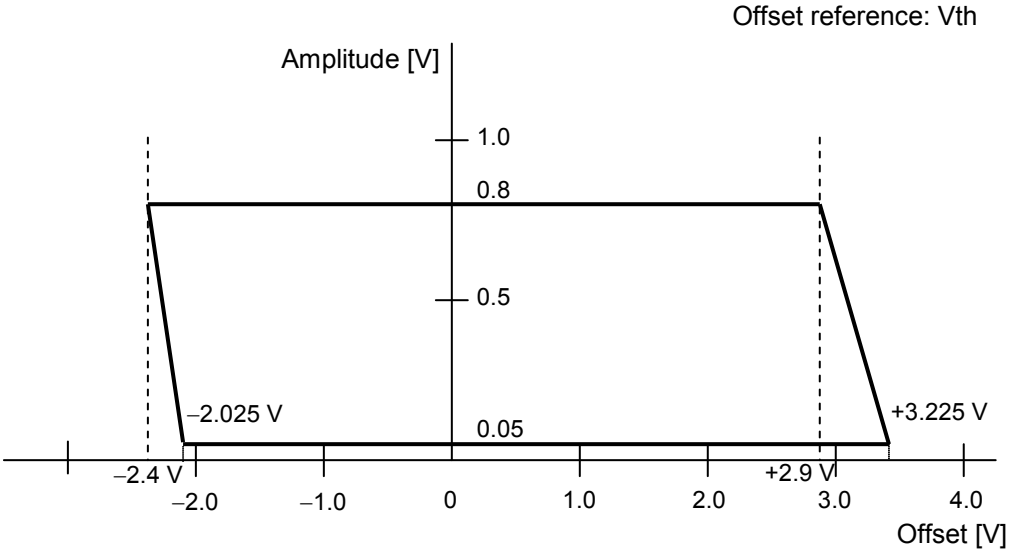


Figure C.1.1.1-2 Setting range of amplitude and offset based on offset reference (Vth) (MU181020A-x10)

(c) Vol

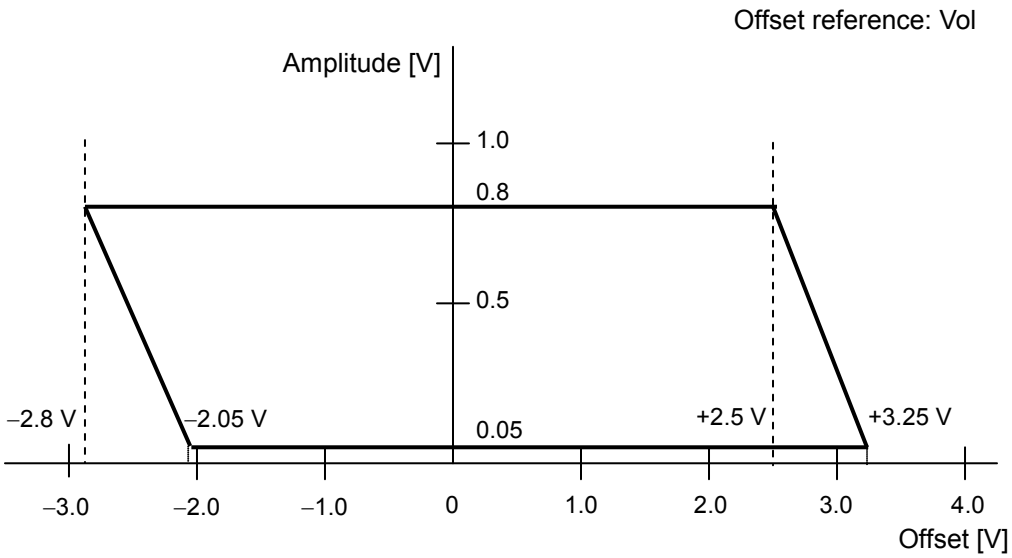


Figure C.1.1.1-3 Setting range of amplitude and offset based on offset reference (Vol) (MU181020A-x10)

C.1.1.2 MU181020A/B-x11 Variable Data Output (0.25 to 2.5 Vp-p)

<Specification>
Amplitude: 0.25 to 2.5 Vp-p
Offset: –2.0 to +3.3 V (Voh)

(a) Voh

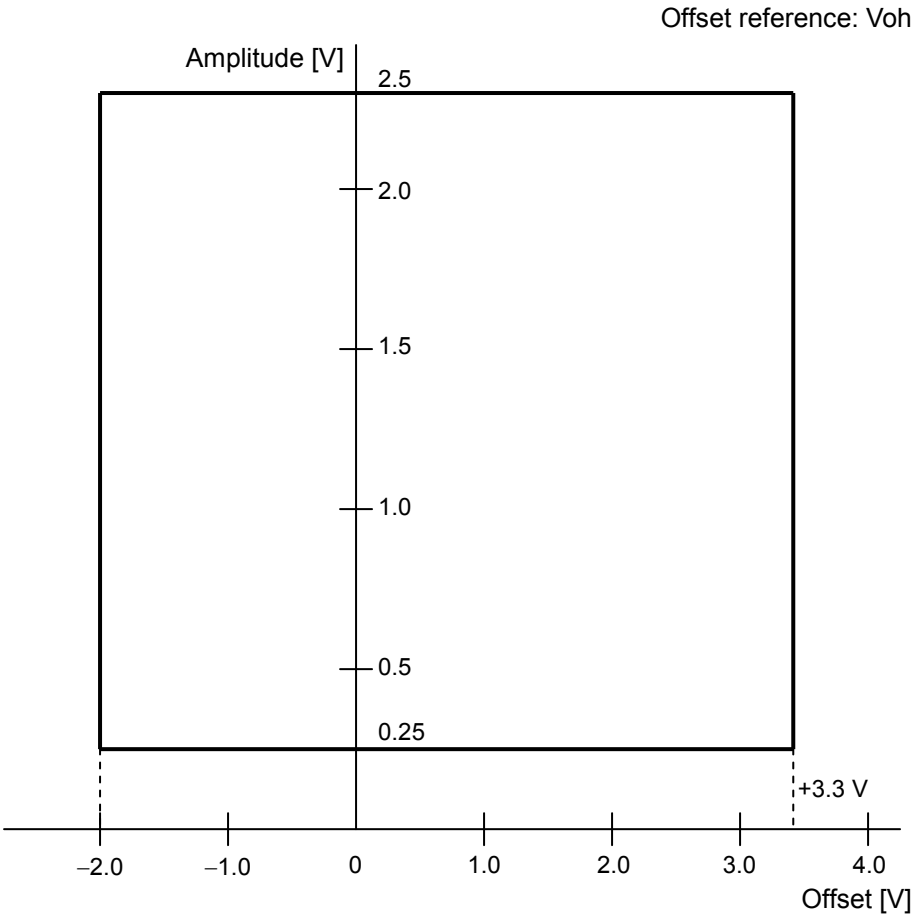


Figure C.1.1.2-1 Setting range of amplitude and offset based on offset reference (Voh) (MU181020A/B -x11)

(b) Vth

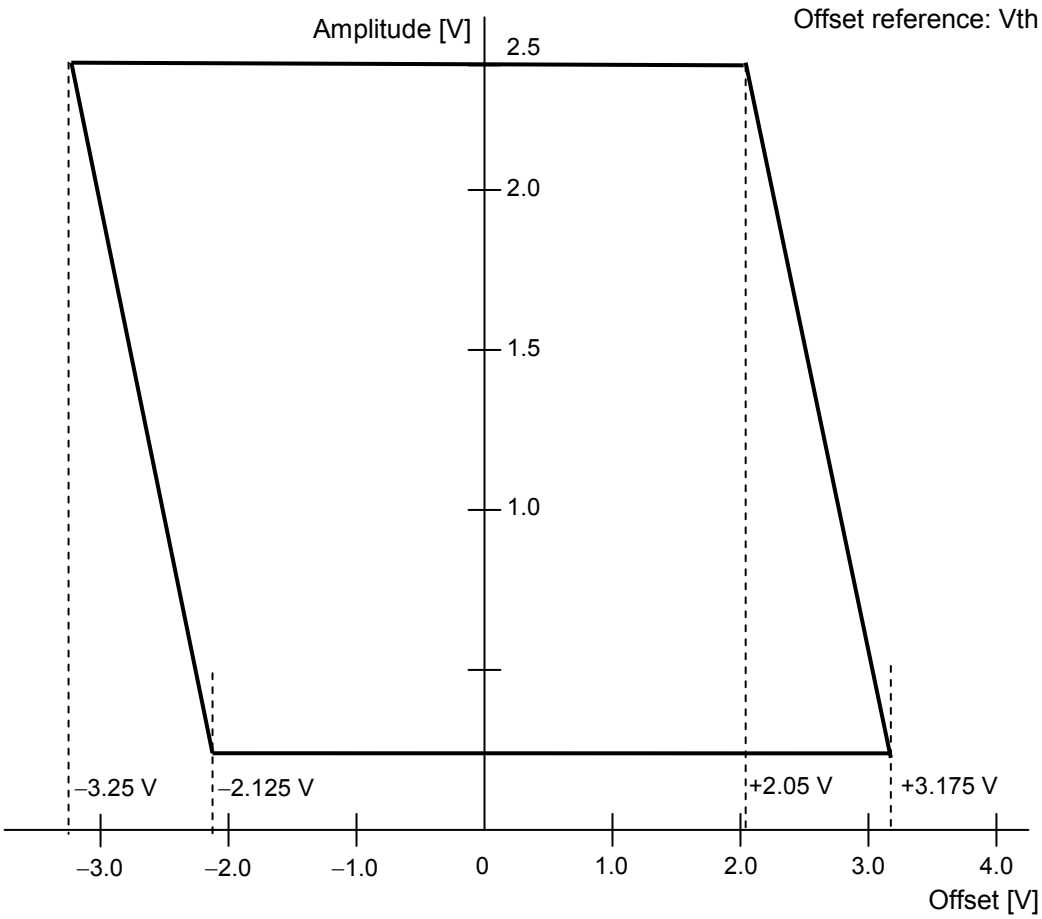


Figure C.1.1.2-2 Setting range of amplitude and offset based on offset reference (Vth) (MU181020A/B -x11)

(c) Vol

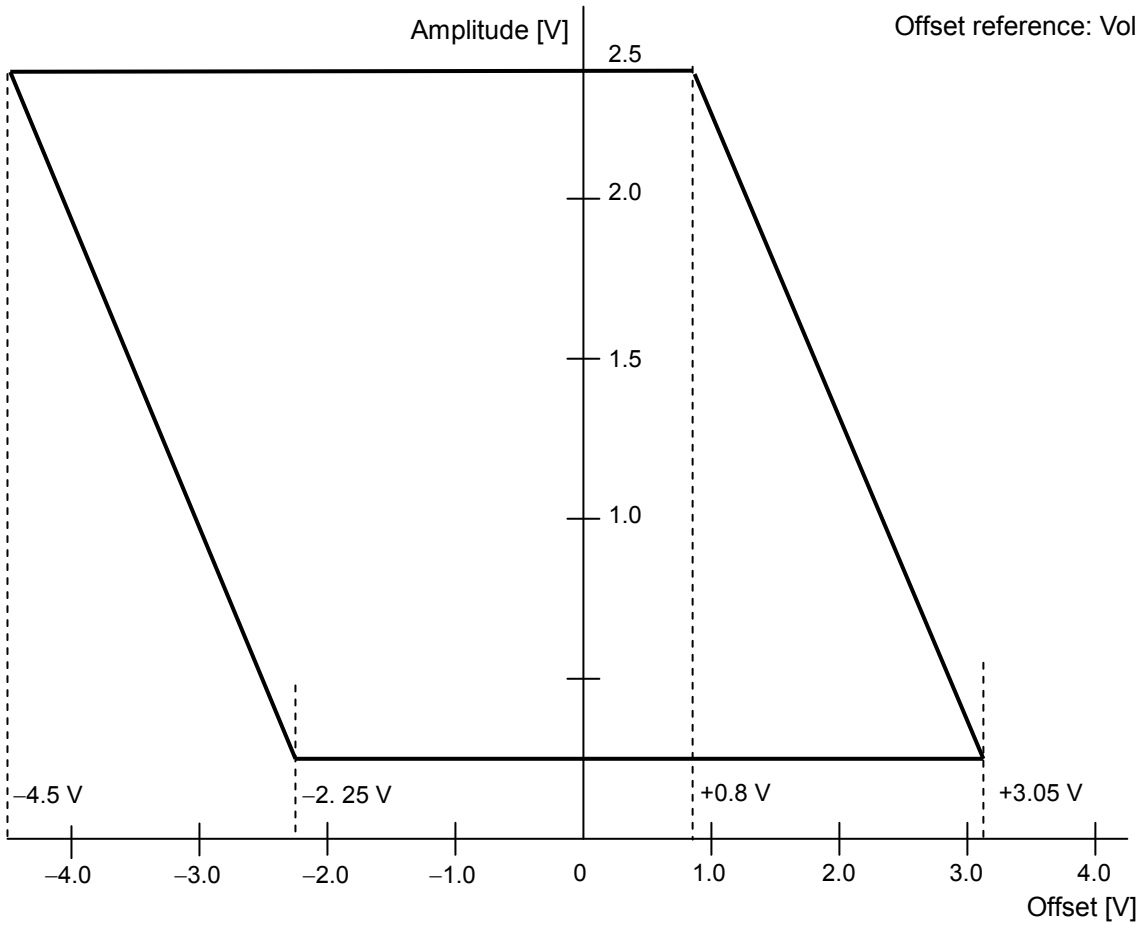


Figure C.1.1.2-3 Setting range of amplitude and offset based on offset reference (Vol) (MU181020A/B -x11)

C.1.1.3 MU181020A/B -x12 High Performance Data Output (0.05 to 2.0 Vp-p)

<Specification>
Amplitude: 0.05 to 2.0 Vp-p
Offset: –2.0 to +3.3 V (Voh)

(a) Voh

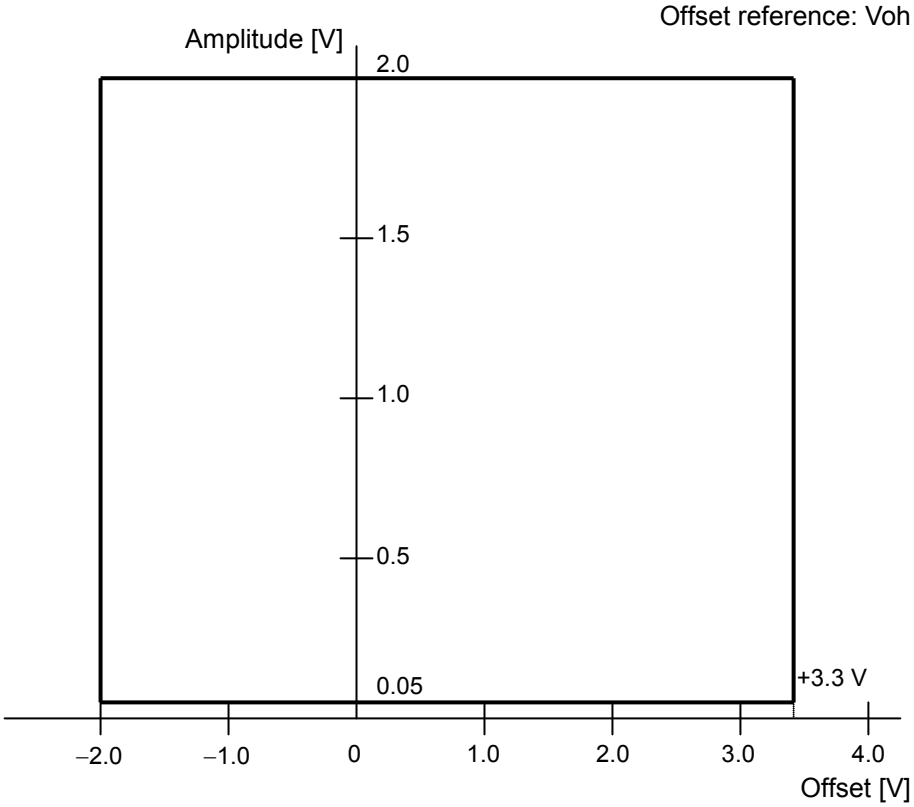


Figure C.1.1.3-1 Setting range of amplitude and offset based on offset reference (Voh) (MU181020A/B -x12)

(b) Vth

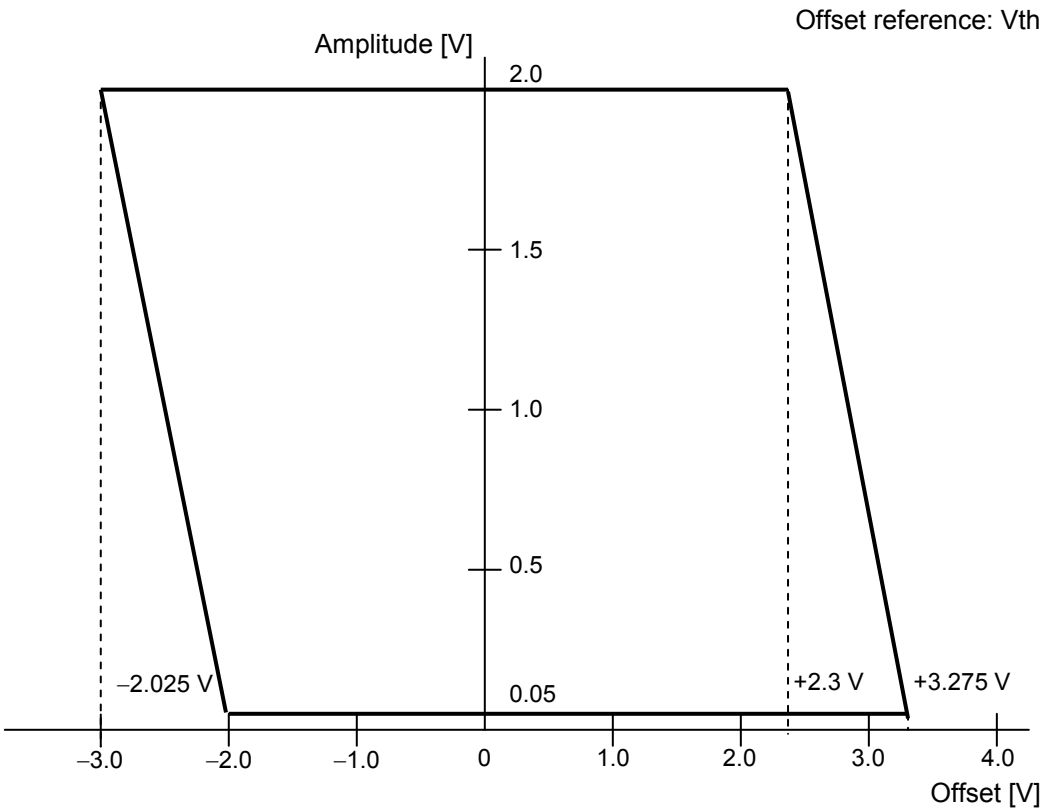


Figure C.1.1.3-2 Setting range of amplitude and offset based on offset reference (Vth) (MU181020A/B -x12)

(c) Vol

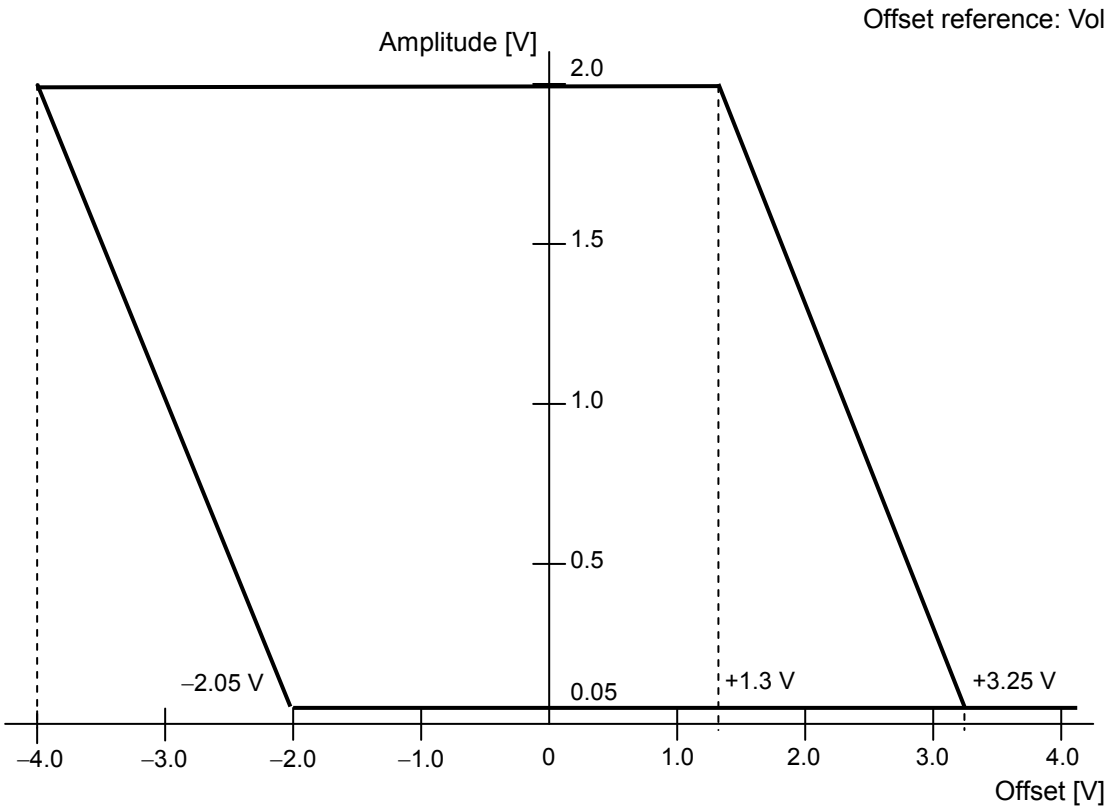


Figure C.1.1.3-3 Setting range of amplitude and offset based on offset reference (Vol) (MU181020A/B -x12)

C.1.1.4 MU181020A/B -x21 1/1 Differential Clock Output (0.1 to 2.0 Vp-p)

<Specification>
Amplitude: 0.1 to 2.0 Vp-p
Offset: –2.0 to +3.3 V (Voh)

(a) Voh

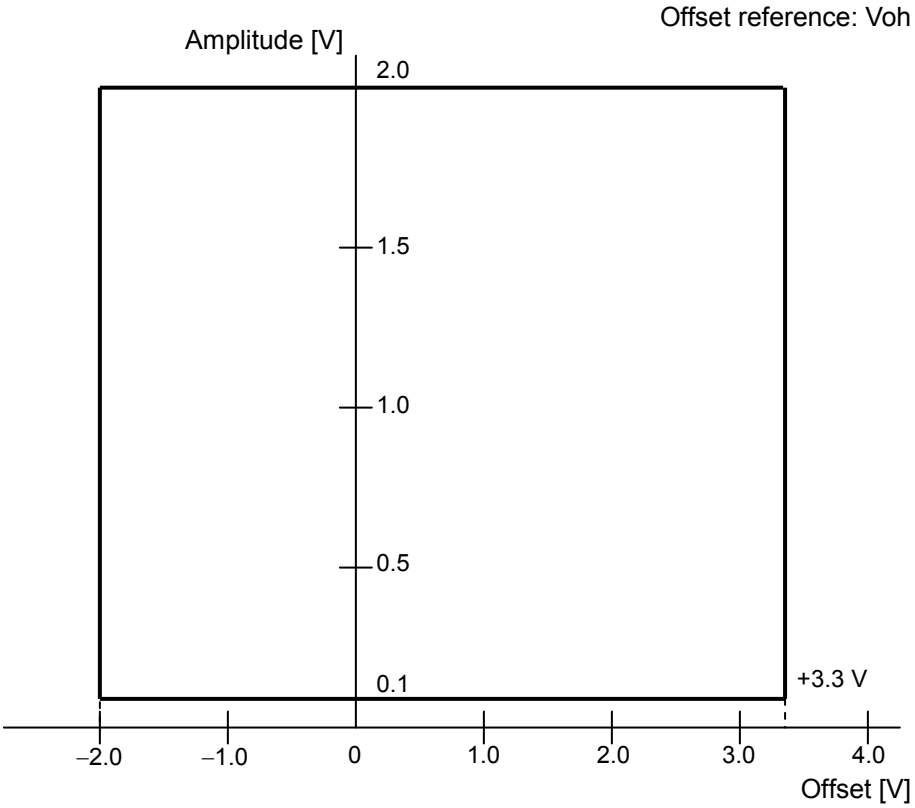


Figure C.1.1.4-1 Setting range of amplitude and offset based on offset reference (Voh) (MU181020A/B -x21)

(b) Vth

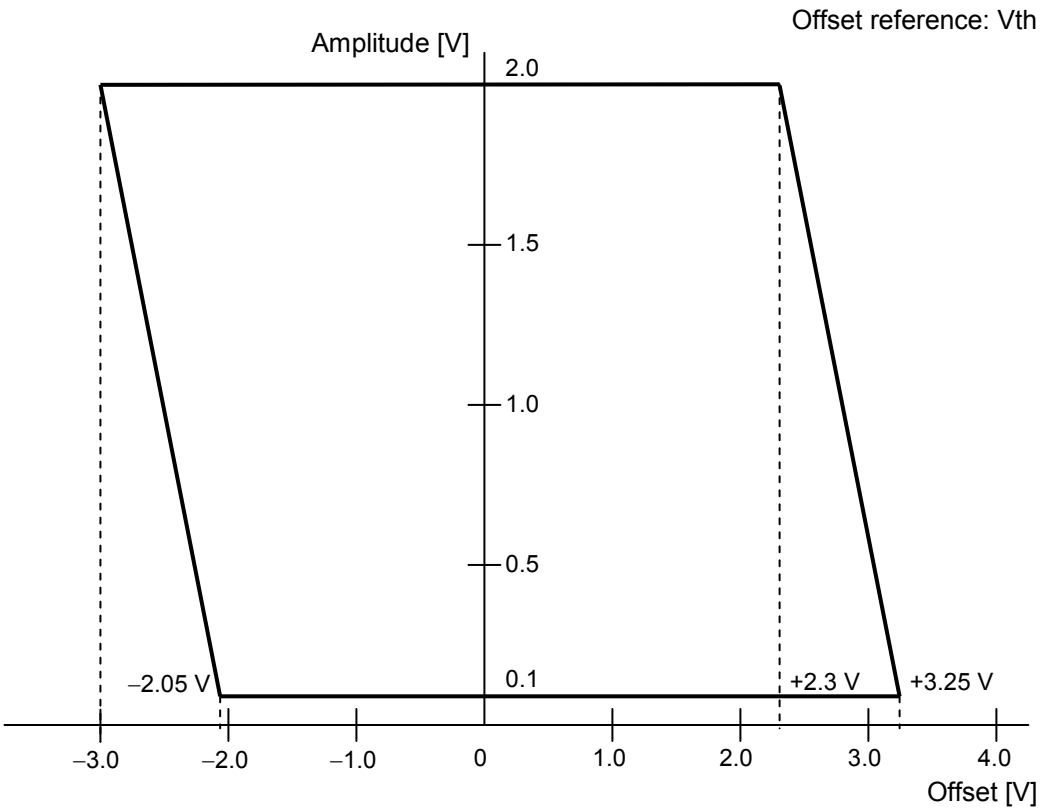


Figure C.1.1.4-2 Setting range of amplitude and offset based on offset reference (Vth) (MU181020A/B -x21)

(c) Vol

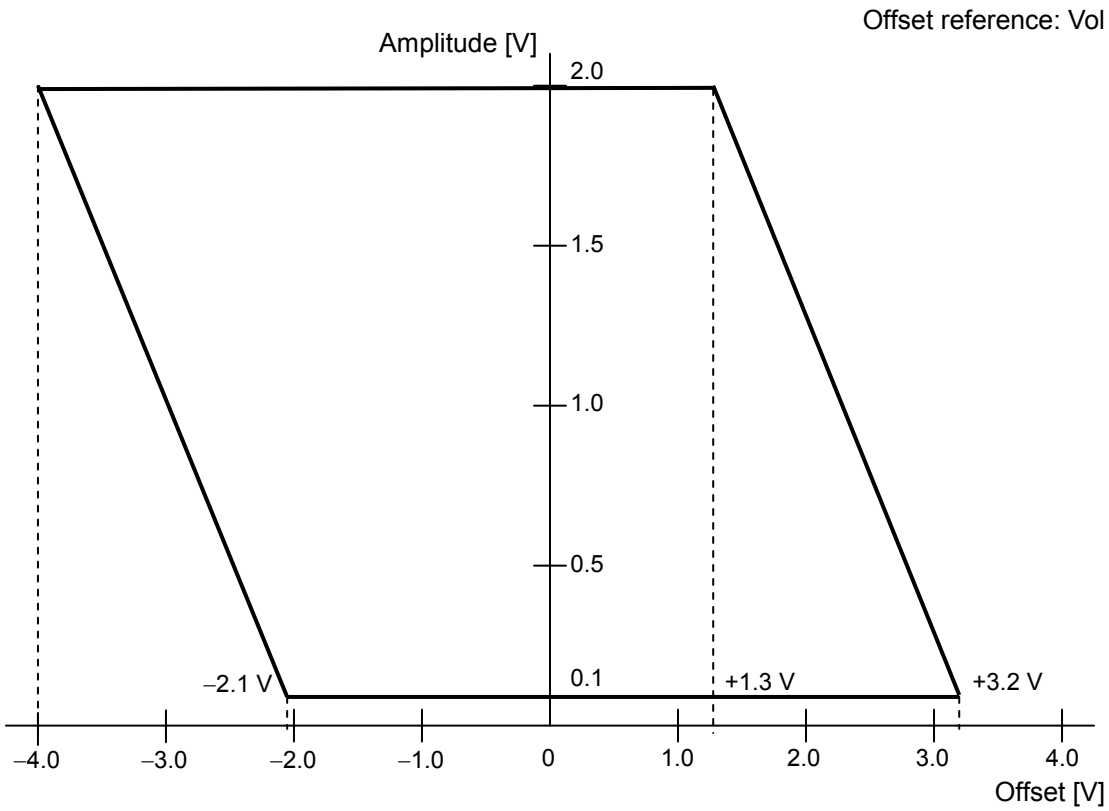


Figure C.1.1.4-3 Setting range of amplitude and offset based on offset reference (Vol) (MU181020A/B -x21)

C.1.1.5 MU181020A/B -x13 Data Output (0.5 to 3.5 Vp-p)

<Specification>
Amplitude: 0.5 to 3.5 Vp-p
Offset: –2.0 to +3.3 V (Voh)

(a) Voh

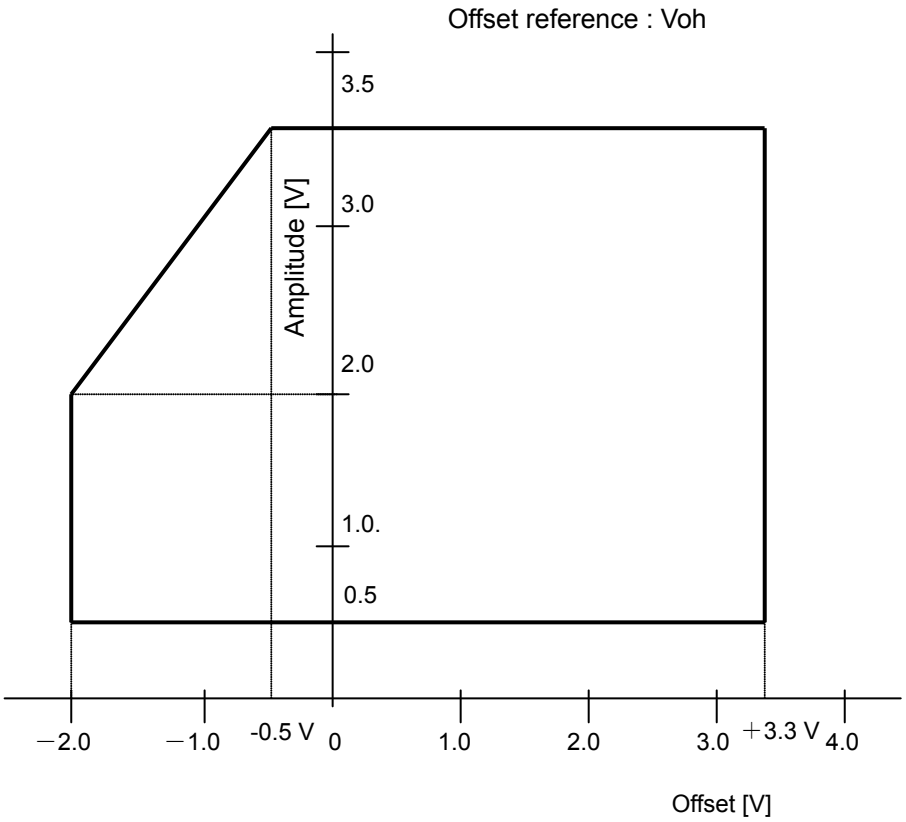


Figure C.1.1.5-1 Setting range of amplitude and offset based on offset reference (Voh) (MU181020A/B -x13)

(b) Vth

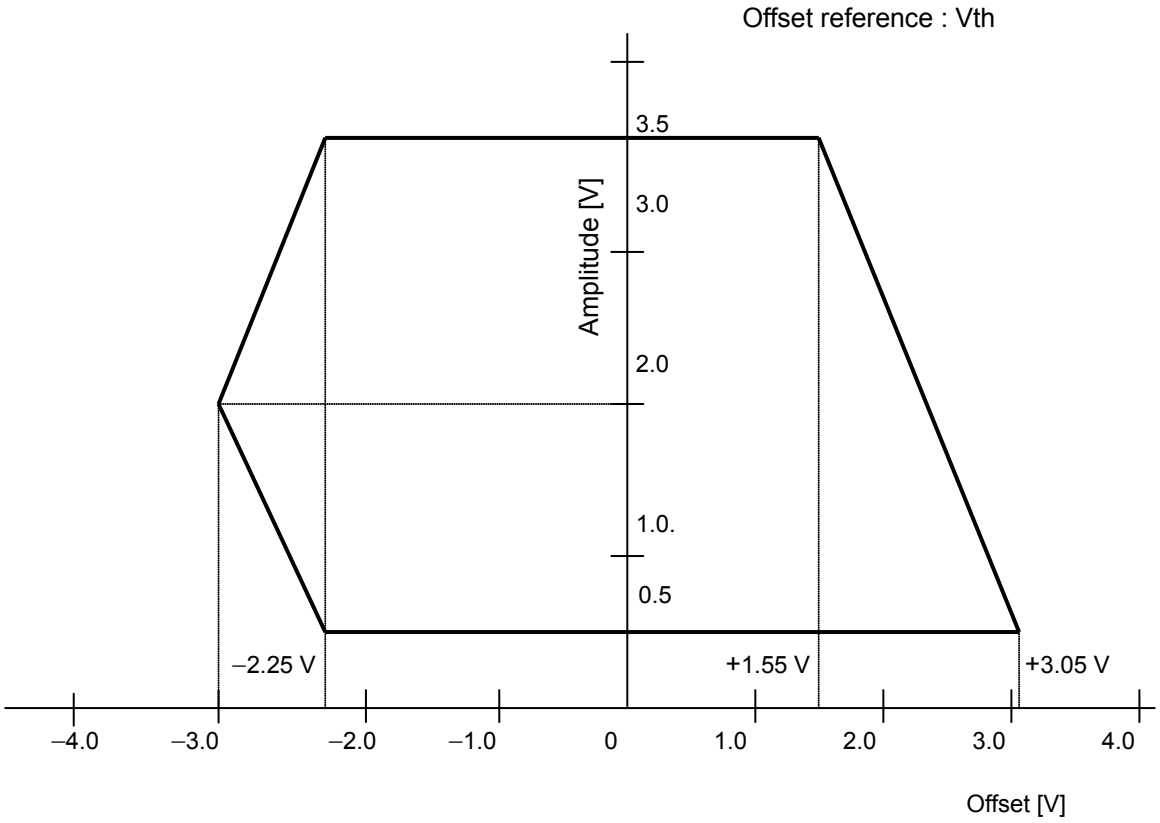


Figure C.1.1.5-2 Setting range of amplitude and offset based on offset reference (Vth) (MU181020A/B -x13)

(c) Vol

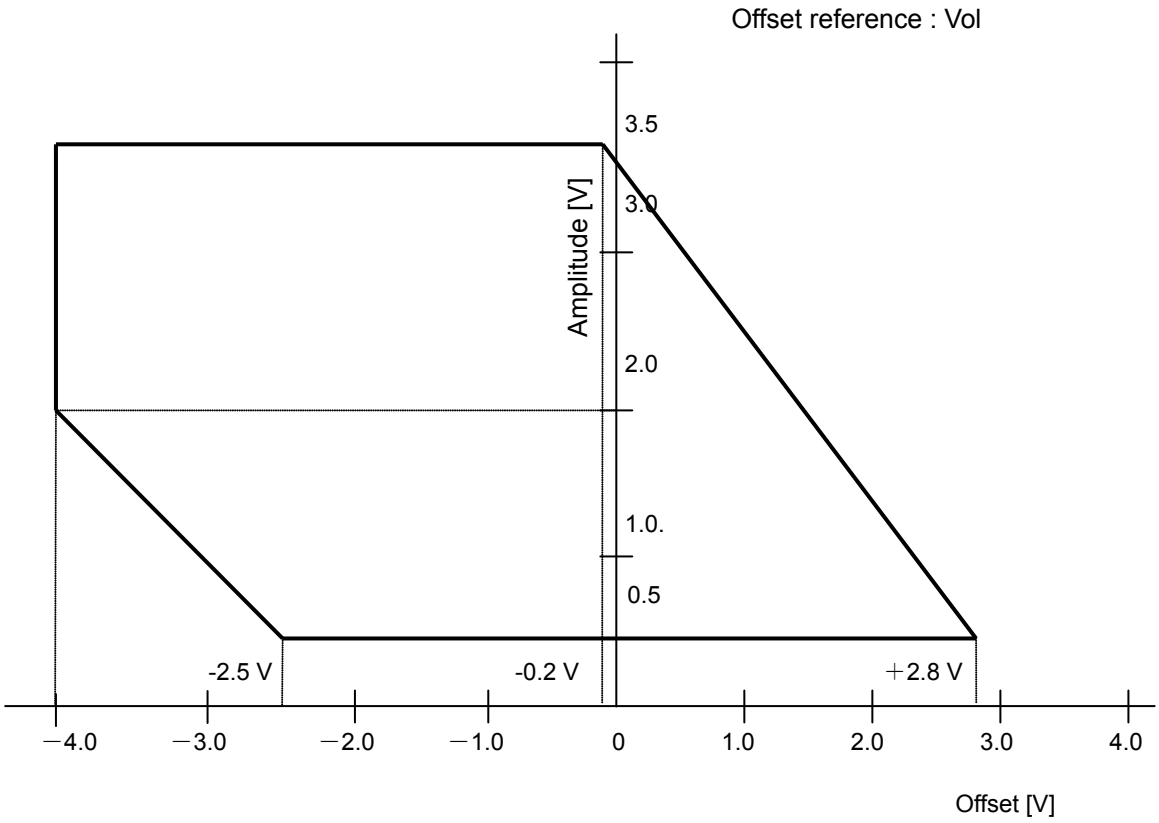


Figure C.1.1.5-3 Setting range of amplitude and offset based on offset reference (Vol) (MU181020A/B -x13)

C.2 Combination Function Configuration

The conditions required to execute the Combination function by using multiple MU181020A modules are described below.

All of the following conditions must be satisfied to execute the Combination function.

Enabling conditions for Combination function

- Two or more MU181020A modules are mounted on one mainframe. (To be mounted from the top Slot1 in order)
- Do not mix the MU181020A and MU181020B.
- Supported installed modules are the MU181020A-002 and MU181020B-002.
- Supported installed modules are the MU181020A-x30 and MU181020B-x30.
- All inserted MU181020A modules must have the same MU181020A-x10/x11/x12/x13 and MU181020B-x11/x12/x13 data output option configuration. Otherwise, no data output option is installed in all inserted MU181020A modules.
- All or none of the inserted MU181020A modules must have MU181020A-x21 and MU181020B-x21 installed therein.
- The mainframe option is either 015 or 016.

In addition, the following restriction is added for the Combination function.

Restriction for Combination function

- The Alternate, Mixed-Alternate and Sequence patterns cannot be used as the test pattern.

C.3 Channel Synchronization Function Configuration

The conditions required to execute the Channel Synchronization function by using multiple MU181020A modules are described below.

All of the following conditions must be satisfied to execute the Channel Synchronization function.

Enabling conditions for Channel Synchronization function

- Two or more MU181020A modules are mounted on one mainframe. The MU181020A modules that are mounted contiguously starting from Slot 1 are enabled.
- Do not mix the MU181020A and MU181020B.
- Supported installed modules are the MU181020A-002 and MU181020B-002.
- Supported installed modules are the MU181020A-x30 and MU181020B-x30.
- All inserted MU181020A modules must have the same MU181020A-x10/x11/x12/x13 and MU181020B-x11/x12/x13 data output option configuration. Otherwise, no data output option is installed in all MU181020A modules.
- All or none of the inserted MU181020A modules must have MU181020A-x21 and MU181020B-x21 installed therein.

C.4 Restrictions on operations when multiple modules are mounted

This section describes the restrictions on operations for executing the Independent function when two or more MU181020A and/or MU181040A/B modules are mounted on the MP1800A/MT1810A. These restrictions apply only when generating Data, Zero-substitution, Mixed, or Sequence patterns, and do not apply when generating PRBS patterns.

Restrictions on Independent function operations

- When two or more MU181020A or MU181040A/B modules are mounted on one MP1800A/MT1810A unit, two frequency bands of 0.1 to 6 Gbit/s and 6 to 12.5 Gbit/s must not be mixed between MU181020A modules and between MU181040A/B modules. However, the frequency band for the MU181020A modules and that for the MU181040A/B modules can exist within the MP1800A/MT1810A.
  Operations at different frequencies are allowed as long as the frequencies fall within the same frequency band.
- When two or more MU181040A/B modules and this equipment are installed in the mainframe, the following modules become the master module for Clock input.

  MP1800A-016 Master Module
  MU181020A, MU181020B: Slot1
  MU181040A, MU181040B: Slot6

  MP1800A-015 or MT1810A-015 Master Module
  MU181020A, MU181020B: Slot1
  MU181040A, MU181040B: Slot1

  However, the following modules become the master module, when the MU181020A/B is installed in Slot1 and 2 and when the MU181040A/B is installed in Slot 3 and 4. (Refer to Figure C.4-3 Restrictions of the case c))
  MU181020A, MU181020B: Slot1
  MU181040A, MU181040B: Slot3

  MP1800A-014 or MT1810A-014 Master Module
  MU181020A, MU181020B: Slot3
- When the module configuration is reconfigured or when the MU181020A/B or MU181040A/B is retrofitted, input the clock signal in the master module of the MU181020A/B and MU181040A/B.

- If the MU181040A-x20 or MU181040B-x20 Clock Recovery option is mounted and selected in an MU181040A/B module, adjust the clock recovery setting bit rate according to the frequency band for the other MU181040A/B modules.

a) MP1800A-016 with four MU181020A and two MU181040A modules mounted

Example:

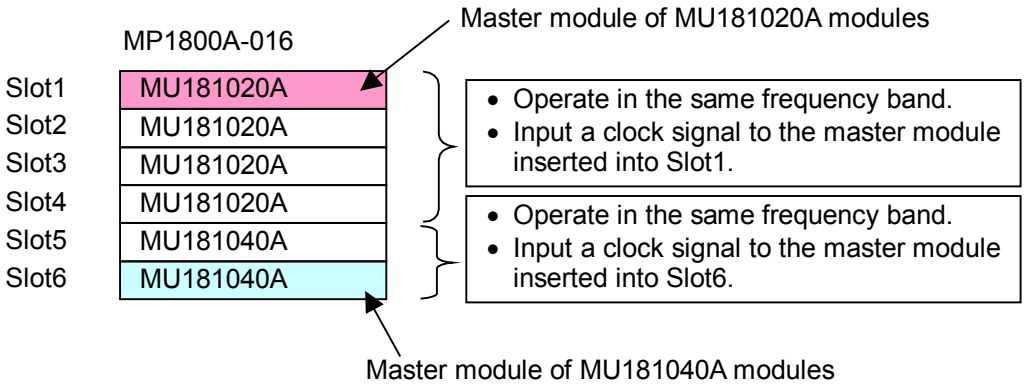


Figure C.4-1 Restrictions of the case a)

b) MP1800A-015/MT1810A-015 with four MU181040A modules mounted

Example:

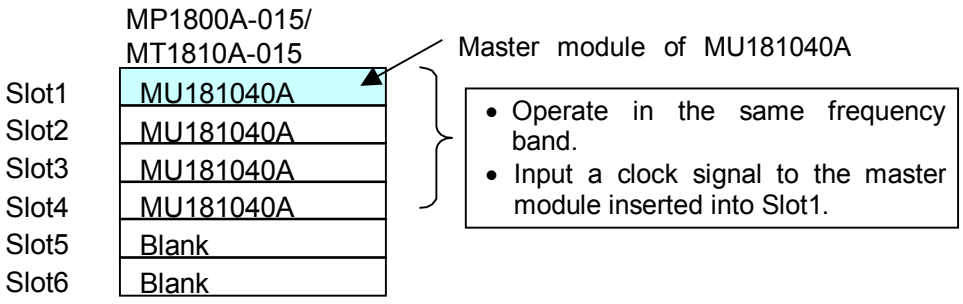


Figure C.4-2 Restrictions of the case b)

c) MP1800A-015/MT1810A-015, with two MU181020A and two MU181040A modules mounted

Example:

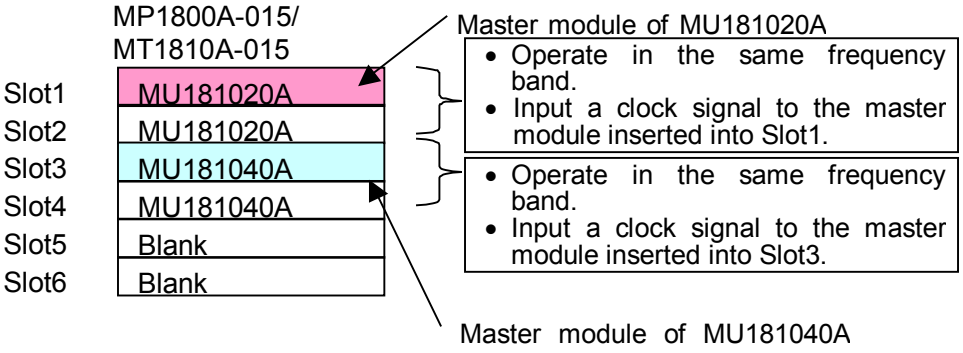


Figure C.4-3 Restrictions of the case c)

When mounting MU181020A or MU181040A/B modules onto the MP1800A/MT1810A, note that the number of modules that can be mounted and the mounting positions (slots) vary depending on the option additionally installed in the MP1800A/MT1810A.
For details, refer to the release note included in this equipment or refer to the Anritsu homepage (http://www.anritsu.com).

C.5 Settings Common in Combination System

When the MU181040A is used in a Combination system, some setting items will apply to all the other modules in the Combination system.

Table C.5-1 shows whether the setting items are common or independent in a Combination system.

Table C.5-1 Common/Independent Setting Items in Combination System

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Output	Data/XData Offset ON/OFF			Independent
	Clock/XClock Offset ON/OFF (MU181020A-x21, MU181020B-x21)			Independent
	Amplitude Offset			Independent
	Data/XData	Tracking		Independent
		Level Guard		Independent
		Level Guard Setup		Independent
			Amplitude limit	Independent
			Offset limit	Independent
		Defined Interface		Independent
			Amplitude	Independent
			Offset switching	Independent
			Offset	Independent
			External ATT Factor	Independent
		Cross Point		Independent
		Delay		Independent
			Calibration	Independent
Output	Clock/XClock (MU181020A –x21, MU181020B– x21)	Tracking		Independent
		Level Guard		Independent
		Level Guard Setup	Amplitude limit	Independent
			Offset limit	Independent
		Defined Interface		Independent
			Amplitude	Independent
			Offset switching	Independent
			Offset	Independent
			External ATT Factor	Independent
		Duty		Independent

Table C.5-1 Common/Independent Setting Items in Combination System (Cont'd)

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Pattern	PRBS			Common
		Number of Rows		Common
		Logic		Common (Pattern Common)
		Mark Ratio		Common (Pattern Common)
		Bit Shift		Common (Common with Mixed Data)
	Zero-Substitution	Number of Rows		Common
		Zero Substitution Length		Common
		Additional Bit		Common
	Data	Data Pattern		Common
	Mixed Data	Logic		Common (Pattern Common)
		Bit Shift		Common (Common with PRBS)
		Block count		Common
		Row Length		Common
		Data Length		Common
		Row count		Common
		PRBS	Pattern	Common
			Mark Ratio	Common (Pattern Common)
		Scramble		Common
		Scramble Setup		Common
		PRBS Sequence		Common
	Pattern Editor	Zoom		Independent
		Block count		Common
		Row Length		Common
		Data Length	Data	Common
			Mixed	Common
		Row count		Common
Error Addition	Error Addition			Common
		Source		Common
		Variation		Common
		Route		Independent
		Error Rate		Common
		When test pattern is Mixed: Row 1		Common

Table C.5-1 Common/Independent Setting Items in Combination System (Cont'd)

Function	Main Category	Sub-Category	Individual Setting Item	Common/ Independent
Misc	Pattern Sequence			Common
		Repeat	Pulse Width	Common
			Delay	Common
		Burst	Source	Common
			Data Sequence	Common
			Enable Period	Common
			Burst Cycle	Common
			Delay	Common
			Pulse Width	Common
	Aux Input			Common
	Aux Output			Independent
		1/N Clock		Independent
		Pattern Sync	PRBS, Zero Substitution, Data: Position	Independent
			Mixed Data: Block No. Row No.	Independent
		Burst Output 2	Delay	Common
			Pulse Width	Common

D.1 Performance Test Record Sheet

D.1.1 MU181020A 12.5Gbit/s

Equipment Name: MU181020A 12.5Gbit/s PPG RF Module

Serial No.:

Ambient Temperature: °C

Relative Humidity: %

Table D.1.1-1 MU181020A Operating Frequency Range

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
MU181020A-001	Internal	9.8 to 12.5 GHz	
	External 1/1		
	External 1/64		
MU181020A-002	External	0.1 to 12.5 GHz	

Table D.1.1-2 MU181020A Data Output

Option Configuration	Item	Specification	Results
MU181020A-001	Output level	H: –0.2 to 0.1 V L: –0.65 to –0.4 V	
	Cross Point	50% ±15%	
	Tr/Tf	Typ. 30 ps (20 to 80%) (≥5 Gbit/s) Typ.40 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 15 ps p–p*	
MU181020A-002	Output level	H: –0.25 to 0.05 V L: –1.4 to –0.85 V	
	Cross Point	50% ±15%	
	Tr/Tf	Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ. 45 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps p–p*	
MU181020A-x10	Amplitude Setting Error	0.05 to 0.8 Vp-p, 2 mV steps ±50 mV±17% (≥0.1 Vp-p) ±25 mV±17% (<0.1 Vp-p)	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	

Table D.1.1-2 MU181020A Data Output (Cont'd)

Option Configuration	Item	Specification	Results
MU181020A-x10 (continued)	Current Limit	Sourcing: 50 mA Sinking: 80 mA	
	Cross Point Adjust	30 to 70%/1% steps (Not independent)	
	Tr/Tf	Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 15 ps p–p (with MU181020A-001 installed) Typ. 10 ps p–p (with MU181020A-002 installed)	
	Waveform Distortion (0 peak)	Typ. ±14% (10 Gbit/s Amplitude: 0.5 to 0.8 Vp–p)	
MU181020A-x11	Amplitude Setting Error	0.25 to 2.5 Vp–p/2-mV steps ±50 mV ±17%	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	
	Current Limit	Sourcing: 50 mA Sinking: 80 mA	
	Cross Point Adjust	30 to 70%/1% steps	
	Tr/Tf	Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 15 ps p–p (with MU181020A-001 installed) Typ. 10 ps p–p (with MU181020A-002 installed)	
	Waveform Distortion (0 peak)	Typ. 25 mV ±6% (at 10 Gbit/s)	
MU181020A-x12	Amplitude Setting Error	0.05 to 2.0 Vp-p, 2 mV steps ±50 mV ±17% (≥0.1 Vp-p) ±25 mV ±17 % (<0.1 Vp-p)	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	

Table D.1.1-2 MU181020A Data Output (Cont'd)

Option Configuration	Specification	Standard	Results
MU181020A-x12	Current Limit	Sourcing : 50 mA Sinking : 80 mA	
	Cross Point Adjust	20 to 80%/1% steps	
	Tr/Tf	Typ. 20 ps (20 to 80%) (Amplitude : 2 Vp-p at 10 Gbit/s and 12.5 Gbit/s) Typ. 25 ps (10 to 90%) (Amplitude : 2 Vp-p at 10 Gbit/s and 12.5 Gbit/s)	
	Total Jitter	Typ. 15 ps p-p (with MU181020A-001 installed) Typ. 8 ps p-p (with MU181020A-002 installed)	
	Waveform Distortion (0 peak)	Typ. ±25 mV ±6 % (10 Gbit/s)	
MU181020A-x13	Amplitude Setting Error	0.5 to 3.5 Vp-p, 2 mV Step ±50 mV ±17%	
	Offset Setting Error	−2.0 to +3.3 Voh/1 mV Step Minimum : −4.0 Vol ±65 mV ±10% of offset (Vth) ±(Amplitude Setting Error/2)	
	Current Limit	Sourcing : 50 mA Sinking : 80 mA	
	Cross Point Adjust	20.0 to 90.0%, 0.1% Step	
	Tr/Tf	Typ. 25 ps (20 to 80%) (Amplitude : 3.5 Vp-p at 10 Gbit/s and 12.5 Gbit/s)	
	Total Jitter	Typ. 8 ps p-p (with MU181020A-001/002 installed at 10 Gbit/s)	
	Waveform Distortion (0 peak)	Typ. 25 mV ±10% (at 10 Gbit/s)	

Table D.1.1-3 MU181020A Clock Output

Option Configuration	Specification	Standard	Results
Without clock option (standard)	Output level	0.5 Vp-p(AC) ±0.25 V (at 8 to 12.5 GHz) 0.65 Vp-p±0.25V (AC) (Fixed) (at 0.1 to 8 GHz)	
	Duty	50% ±15%	
	Tr/Tf	Typ. 30 ps (20 to 80%) (at 12.5 GHz, 10 GHz)	
	Total Jitter	Typ. 2ps (RMS) (with MU181020A-001 installed) Typ. 1ps (RMS) (with MU181020A-002 installed)	
MU181020A-x21	Output level	100 mV to 2.0 Vp–p/2-mV steps ±70 mV ±17% (≥0.2 Vp-p) ±50 mV ±17% (<0.2 Vp-p)	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	
	Duty	–25 to 25/1 step (No Unit) (Not independent)	
	Tr/Tf	Typ. 24 ps (20 to 80%)	
	Total Jitter	Typ. 2 ps (RMS)* (with MU181020A-001 installed) Typ. 1 ps (RMS)* (with MU181020A-002 installed)	

*: The jitter specification value is defined assuming that an oscilloscope with residential jitter less than 200 fs (RMS) is used.

Table D.1.1-4 MU181020A Delay

Option Configuration	Specification	Standard	Results
MU181020A-x30	Phase Setting Range	–1000 to +1000 mUI	
	Phase Setting Resolution	1 mUI	
	Phase Setting Error	Typ. 20 mUI (after calibration)	

D.1.2 MU181020B 14Gbit/s

Equipment Name: MU181020B 14Gbit/s PPG RF Module

Serial No.:

Ambient Temperature: °C

Relative Humidity: %

Table D.1.2-1 Operating Frequency Range

Option Configuration	Signal Source	Operating Frequency Range Specification	Results
MU181020B-002	External	0.1 to 14 GHz	
MU181020B-003	External	0.1 to 14.05 GHz	
MU181020B-005	External	0.1 to 14.1 GHz	

Table D.1.2-2 Data Output

Option Configuration	Item	Specification	Results
MU181020B-002 or MU181020B-003 or MU181020B-005	Output level	H: –0.25 to 0.05 V L: –1.4 to – 0.85 V	
	Cross Point	50% ±15%	
	Tr/Tf	Typ. 35 ps (20 to 80%) (≥5 Gbit/s) Typ. 45 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps p–p*	
MU181020B-x11	Amplitude Setting Error	0.25 to 2.5 Vp–p/2-mV steps ±50 mV ±17%	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	
	Current Limit	Sourcing: 50 mA Sinking: 80 mA	
	Cross Point Adjust	30 to 70%/1% steps	
	Tr/Tf	Typ. 28 ps (20 to 80%) (≥5 Gbit/s) Typ. 35 ps (20 to 80%) (<5 Gbit/s)	
	Total Jitter	Typ. 10 ps p–p*	
	Waveform Distortion (0 peak)	Typ. 25 mV ±6% (at 10 Gbit/s)	

Table D.1.2-2 Data Output (Cont'd)

Option Configuration	Specification	Standard	Results
MU181020B-x12	Amplitude Setting Error	0.05 to 2.0 Vp-p, 2 mV steps ±50 mV ±17% (≥0.1 Vp-p) ±25 mV ±17 % (<0.1 Vp-p)	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	
	Current Limit	Sourcing : 50 mA Sinking : 80 mA	
	Cross Point Adjust	20 to 80%/1% steps	
	Tr/Tf	Typ. 20 ps (20 to 80%) (Amplitude : 2 Vp-p at 10 Gbit/s, 12.5 Gbit/s and 14 Gbit/s) Typ. 25 ps (10 to 90%) (Amplitude : 2 Vp-pat 10 Gbit/s, 12.5 Gbit/s and 14 Gbit/s)	
	Total Jitter	Typ. 8 ps p–p*	
	Waveform Distortion (0 peak)	Typ. ±25 mV ±6 % (10 Gbit/s)	
MU181020B-x13	Amplitude Setting Error	0.5 to 3.5 Vp-p, 2 mV Step ±50 mV ±17%	
	Offset Setting Error	–2.0 to +3.3 Voh/1 mV Step Minimum : –4.0 Vol ±65 mV ±10% of offset (Vth) ±(Amplitude Setting Error/2)	
	Current Limit	Sourcing : 50 mA Sinking : 80 mA	
	Cross Point Adjust	20.0 to 90.0%, 0.1% Step	
	Tr/Tf	Typ. 25 ps (20 to 80%) (Amplitude : 3.5 Vp-p at 10 Gbit/s, 12.5 Gbit/s and 14 Gbit/s)	
	Total Jitter	Typ. 8 ps p-p* (at 10 Gbit/s)	
	Waveform Distortion (0 peak)	Typ. 25 mV ±10% (at 10 Gbit/s)	

Table D.1.2-3 Clock Output

Option Configuration	Specification	Standard	Results
Without clock option (standard)	Output level	0.5 Vp-p(AC) +0.4 V/–0.25 V (at 8 to 14 GHz) 0.65 Vp-p ±0.25V (AC) (Fixed) (at 0.1 to 8 GHz)	
	Duty	50% ±15%	
	Tr/Tf	Typ. 30 ps (20 to 80%) (at 14 GHz, 12.5GHz, 10 GHz)	
	Total Jitter	Typ. 1ps (RMS) *	
MU181020B-x21	Output level	0.1 V to 2.0 Vp–p/2-mV steps ±70 mV ±17% (≥0.2 Vp-p) ±50 mV ±17% (<0.2 Vp-p)	
	Offset Setting Error	–2.0 to +3.3 Voh/1-mV steps ±65 mV ±10% of Offset (Vth) ± (Amplitude Setting Error/2)	
	Duty	–25 to 25/1 step (No Unit) (Not independent)	
	Tr/Tf	Typ. 24 ps (20 to 80%)	
	Total Jitter	Typ. 1 ps (RMS)*	

*: The jitter specification value is defined assuming that an oscilloscope with residential jitter less than 200 fs (RMS) is used.

Table D.1.2-4 Delay

Option Configuration	Specification	Standard	Results
MU181020B-x30	Phase Setting Range	–1000 to +1000 mUI	
	Phase Setting Resolution	1 mUI	
	Phase Setting Error	Typ. 20 mUI (after calibration) (with MU181020B-x30 installed)	

Appendix E Preparing to Use Unit Sync Function

E.1 Preparing to Use Unit Sync Function

This section explains the connections for using the Unit Sync function and the procedure for adjusting the output pattern sync. These examples explain use of four MP1800A main-frame units each containing four MU181020A/B PPG modules.

Setup:
Four MP1800A main-frame units
Sixteen MU181020A/B modules (four modules in each main frame)
12.5G Channel Synchronization setting
PRBS15 pattern setting

E.1.1 Connections when Using Unit Sync

This section explains the connections for using the Unit Sync function.

Use of the Unit Sync function requires connecting the Gating Output connector of the main frame with the AUX Input connector. Connect the Gating Output and AUX Input connectors of each module as described below.
Refer to Section 3.1 “Panel Layout” for the names and functions of connectors.

1. The reference MP1800A is defined as the master unit and the other three are defined as slave units.
2. The Gating Output connector of the MU181020A/B module in Slot 1 of the master MP1800A is connected to the AUX Input connector of the same module (Figure E.1.1-1).
3. The Gating Output connectors of the MU181020A/B modules in Slot 2 to Slot 4 of the master MP1800A are connected to the AUX Input connectors of the MU181020A/B modules installed in Slot 1 of each slave MP1800A (Figure E.1.1-1 and Figure E.1.1-2).

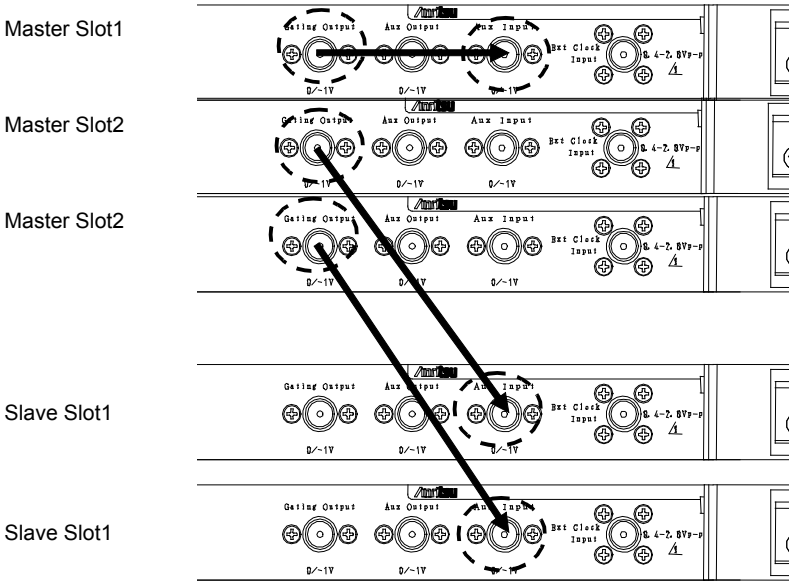


Figure E.1.1-1 MU181020A/B Connection Examples

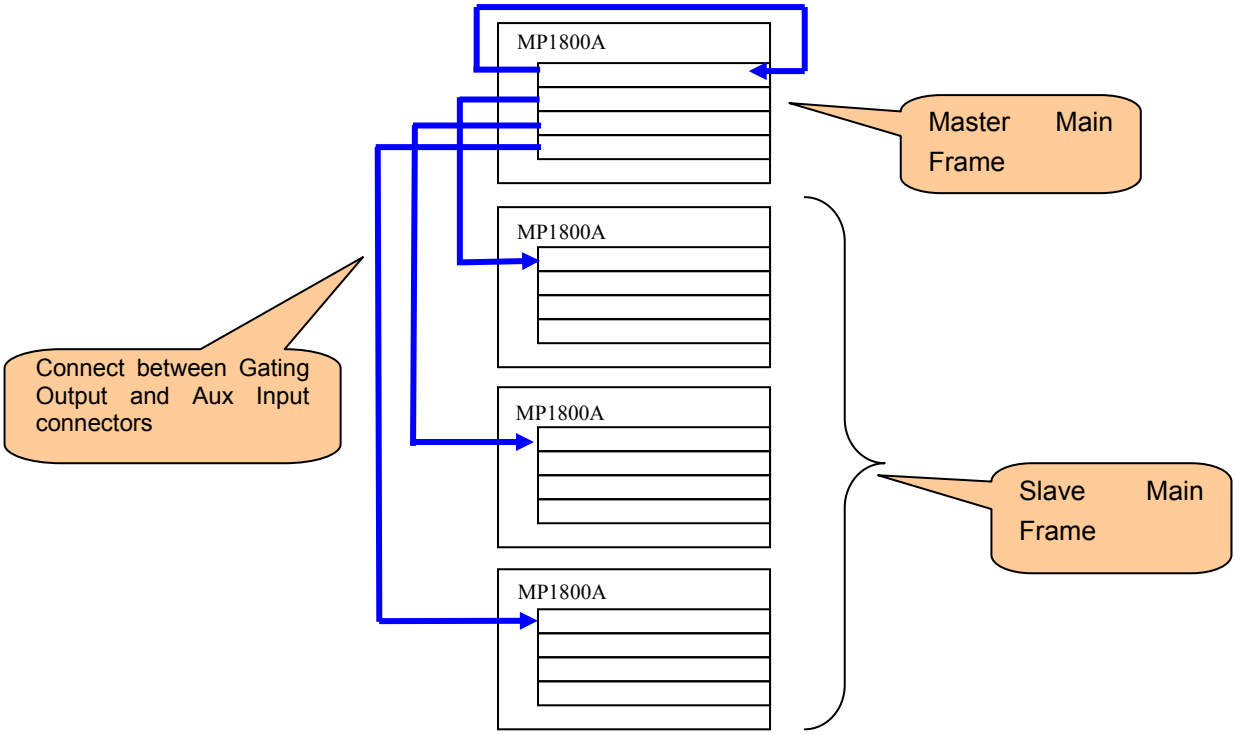


Figure E.1.1-2 Connection Example for Four MP1800A Main Frame Units

E.1.2 Pattern Sync Adjustment Procedure

Use of the Unit Sync functions requires adjustment to compensate for errors caused by differences in the lengths of cables making connections between the main frames and by the specified error (±200 mUI) of the Multi Channel function. After connecting the main frames, set the Unit Sync function to ON and adjust the pattern synchronization between main frames using the following procedure.
See Chapter 5 “Operation Method” for details of each MU181020A/B setting.

1. Input the clock used by each main frame and module.
   Input a stabilized clock. This adjustment is necessary when the clock input is interrupted or changed.
2. Set the pattern at each main frame or each module.
   Synchronization between main units has an error of ±256 bits. This adjustment requires use of a pattern longer than 513 bits.
3. Press [Unit Sync Output] at the master MP1800A.
   If the pattern is changed, it is necessary to synchronize the pattern output by pressing the [Unit Sync Output] button.
4. While monitoring the data output of Slot 1 to Slot 4 of each main frame with an oscilloscope, adjust the [Delay] setting at the [Output] tab for each slot to minimize the bit drift. Make this adjustment at all four main frames (Figure E.1.2-1 and Figure E.1.2-2).
5. Set the signal delay time output from the Gating Output of the MU181020A/B in Slot 2 to Slot 4 of the master MP1800A using the [Delay] setting at [Pattern Sequence] of the [Misc] tab for each slot, and then press the [Unit Sync Output] button. At this time, adjust the Delay value to minimize the bit drift using while monitoring the data output of Slot 1 of each main frame with an oscilloscope.
6. While monitoring the data of Slot 1 of each main frame with an oscilloscope, use the [Unit Offset] setting of the [Output] tab for any of Slot 1 to Slot 4 of each main frame to minimize the bit drift (Figure E.1.2-3 and Figure E.1.2-5).

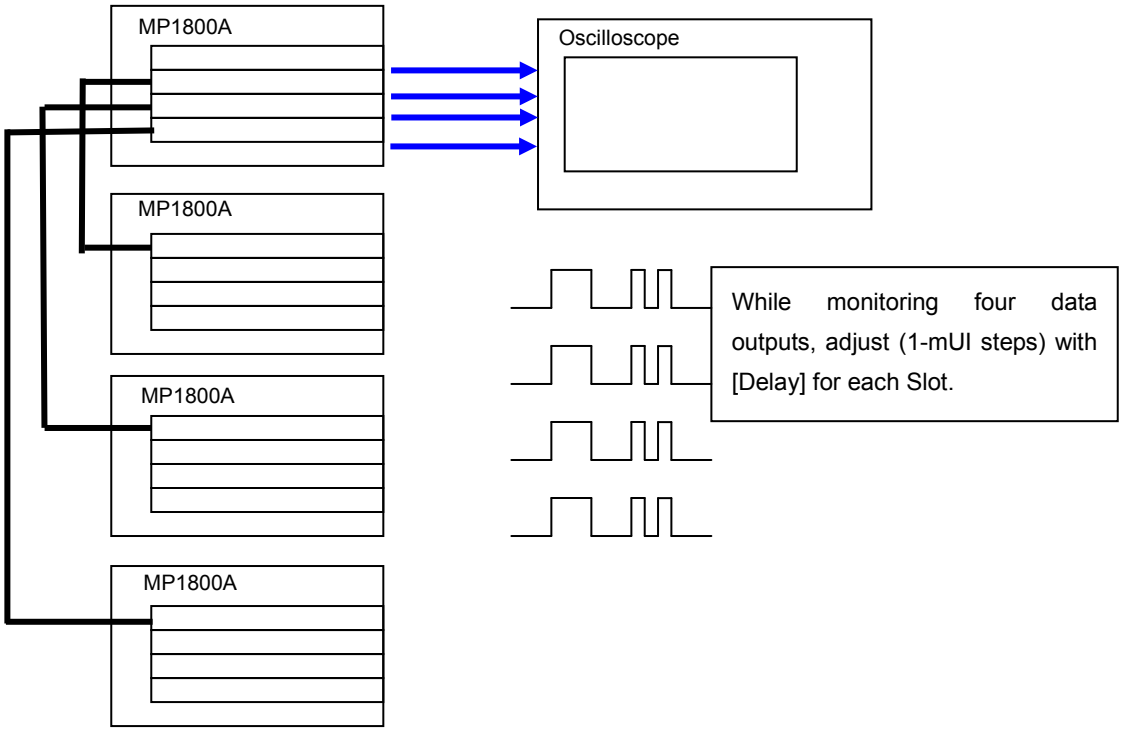


Figure E.1.2-1 Adjusting Output Pattern between Modules

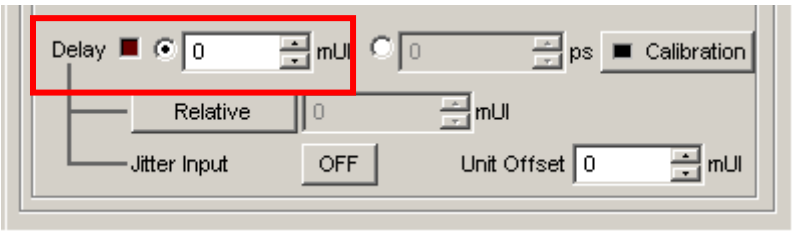


Figure E.1.2-2 Delay Setting Screen

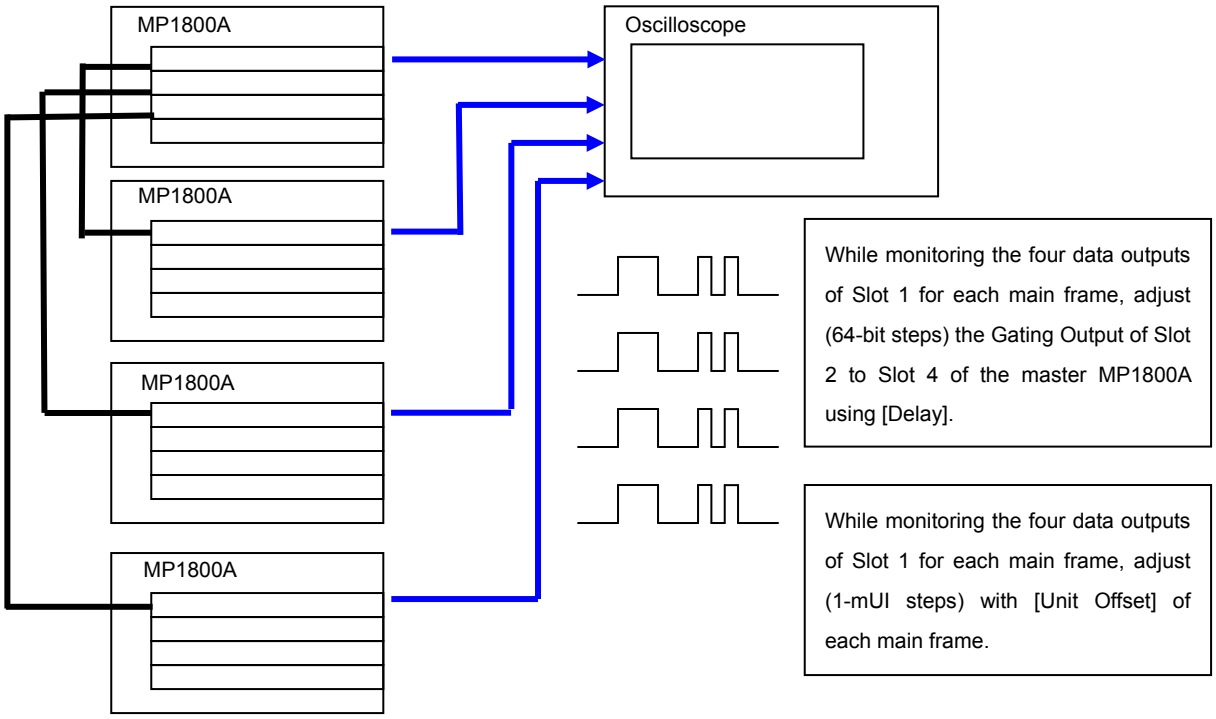


Figure E.1.2-3 Adjusting Output Pattern between Main Units

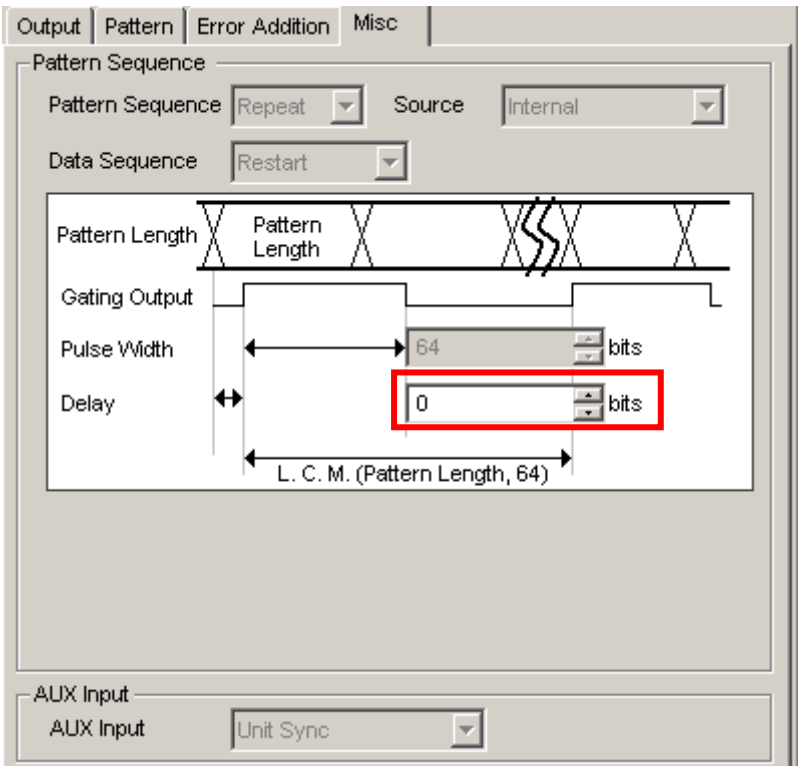


Figure E.1.2-4 Gating Output Delay Setting Screen

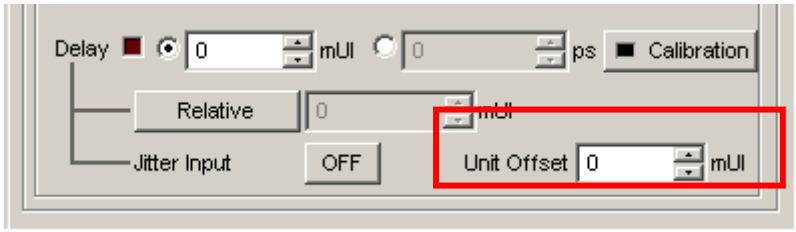


Figure E.1.2-5 Unit Offset Setting Screen